Compound Semiconductor Based Integrated Optical Devices for OFC

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Outline

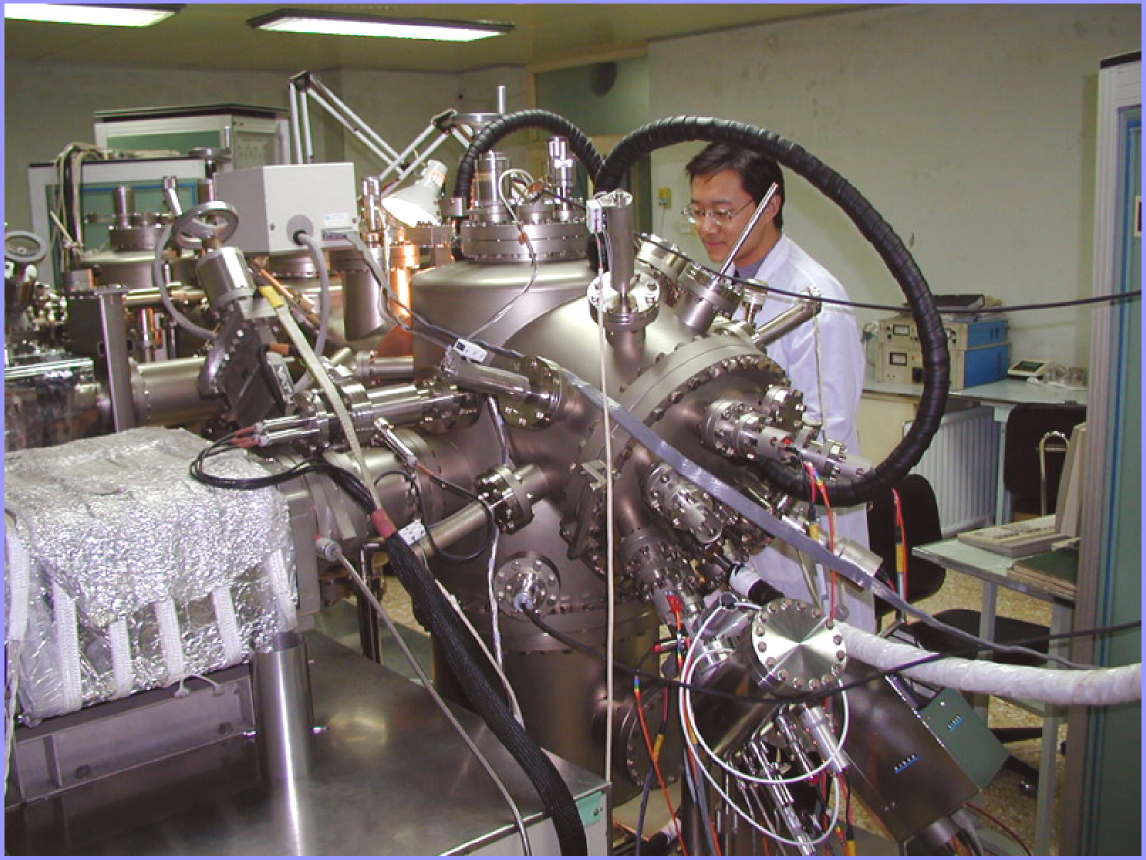
- Brief Introduction
- Device Structure of Recent Work
- Fabrication Technologies
- Characteristics
- Fabrication and Characteristics of Module for 40 Gb/s Applications

Brief Introduction of Our State Key Lab

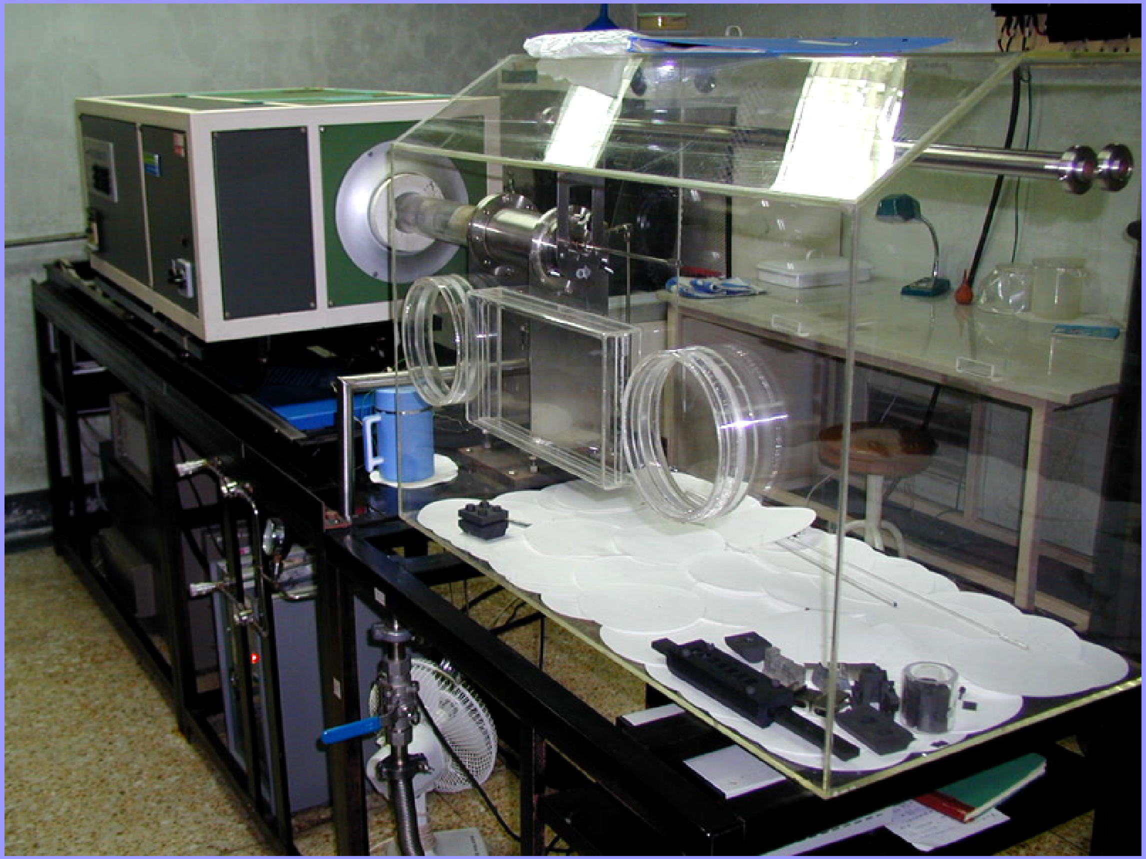
- What are the State Key Labs
- We are Jointed by THU, Jilin Univ., and Semiconductor Institute of CAS
- We are among the best in IT area
- Main research subjects in THU
  - Optoelectronic Materials and Devices
  - Components Based on Fiber
  - High Speed Optical Fiber Transmission and Network Technologies

Molecular Beam Epitaxy

Molecular Beam Epitaxy



Liquid Phase Epitaxy



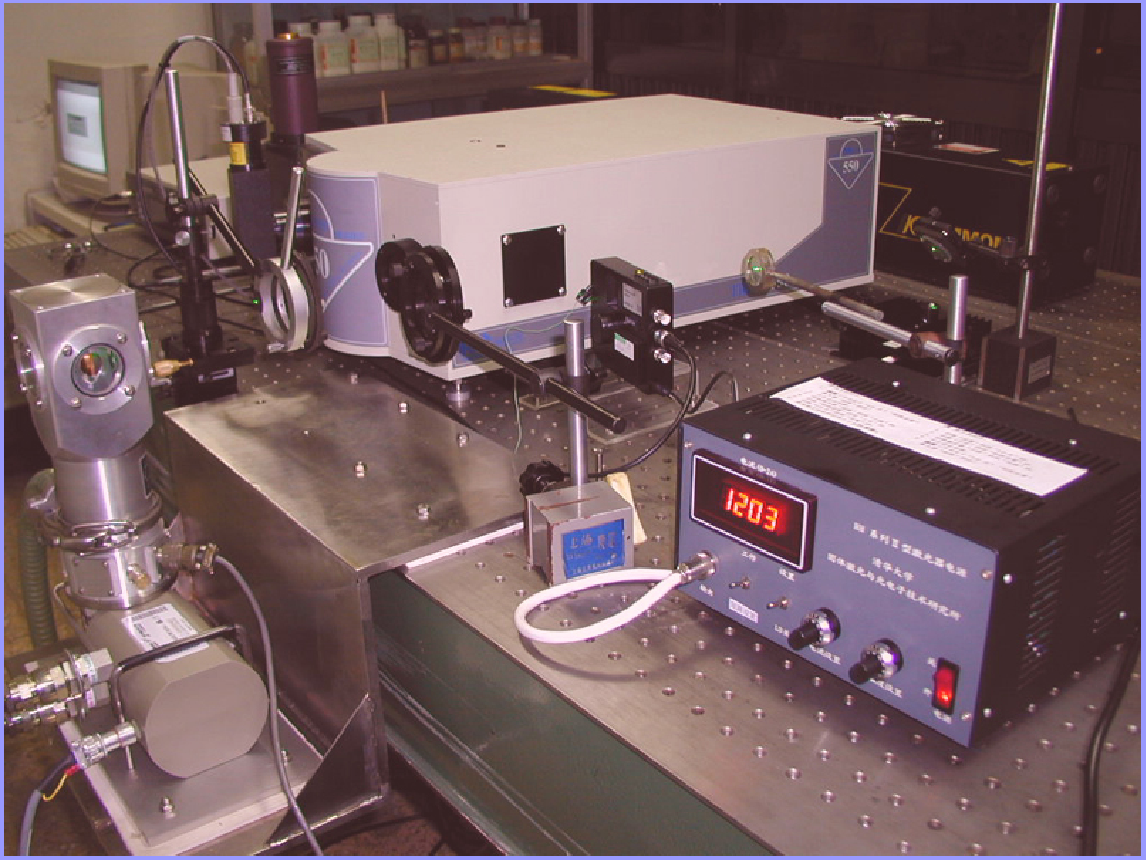
MOCVD System for GaN

Laboratory Facilities

- Wafer Characterization
  - High Resolution X-Ray Diffraction (HR-XRD)
    - Structural characteristics of epitaxial layers
  - Photoluminescence (PL)
    - Optical properties of wafer
  - Hall Measurement
    - Electronic characteristics of materials

High Resolution XRD

Photoluminescence



Hall Measurement

Laboratory Facilities

- Chip Processing
  - Lithography
    - Pattern and mask forming
  - Plasma-Enhanced CVD (PECVD)
    - SiO_2 and Si_xN film deposition
  - Inductively Coupled Plasma (ICP)
    - Dry etching of GaAs, InP, and GaN materials

Lithography

PECVD System

ICP Dry-Etching System

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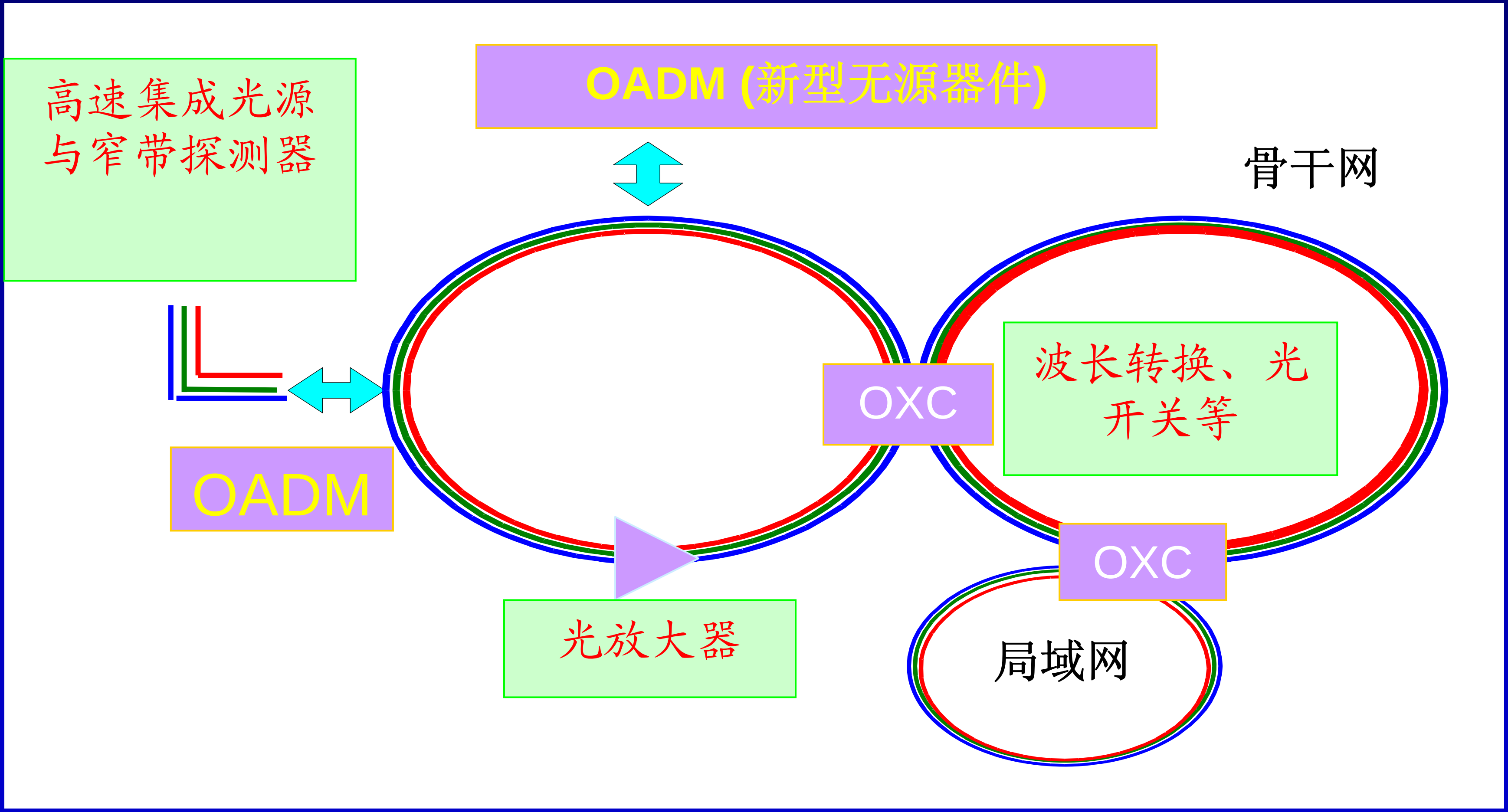
光纤通信网络中的的有源器件



光纤网络中的关键有源器件

- 各种光源
  - 低成本、高可靠激光器（**FP-LD，VCSEL**）
  - 直接调制的**DFB-LD**
  - **DFB-LD / EA**调制器集成光源
  - 波长可调谐与波长可选择激光器
- 高速波导探测器
- 半导体光放大器与波长转化器件

低成本、高可靠半导体激光器

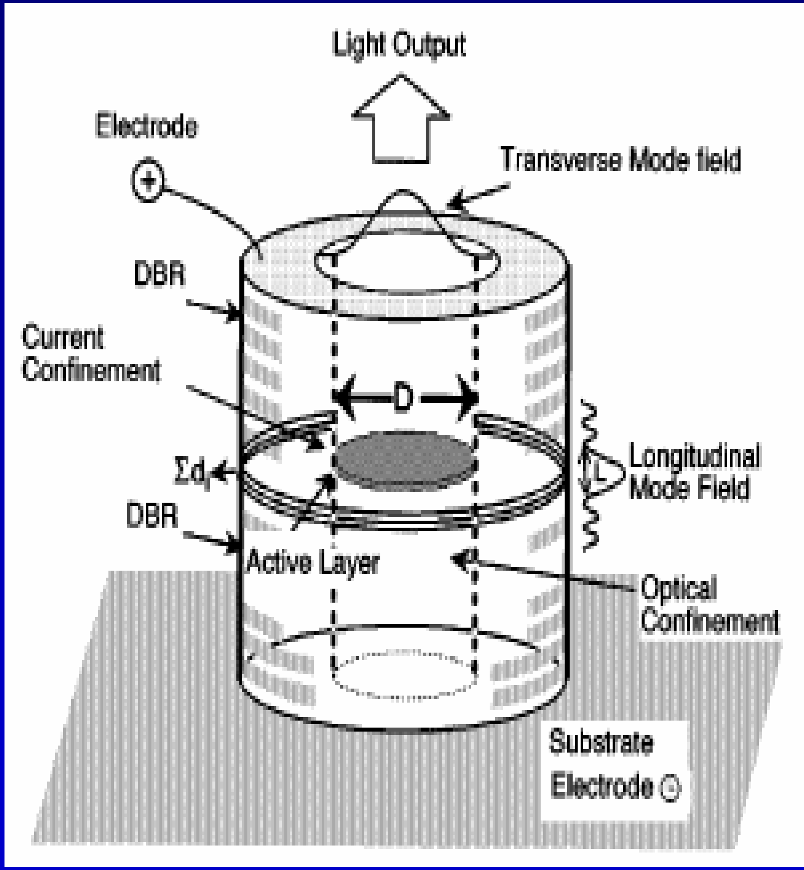
- 应用领域
  - 局域网（Access network）
  - 城域网（Metropolitan transmission）
  - Bit rate: 155 MB/s (FP-LDs) ~ 10 Gb/s (DFB-LDs)
- 低成本、高可靠的要求
  - 宽工作温度范围
  - 高成品率与低制造成本
  - 易于封装

FP-LD及其努力方向

- **Full-Wafer**的制造技术：端面刻蚀技术与端面镀膜技术
- 提高温度特性的途径：**AlGaInAs**激光器与高特征温度

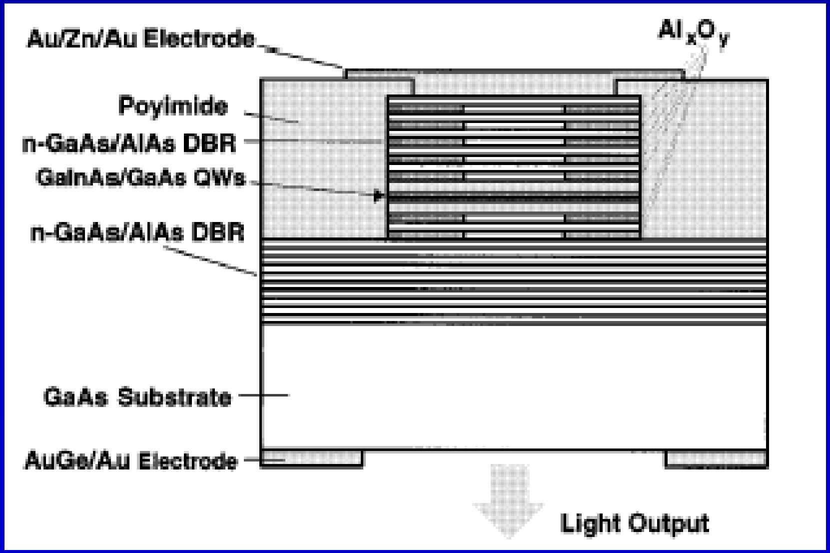
垂直腔面发射激光器的优点

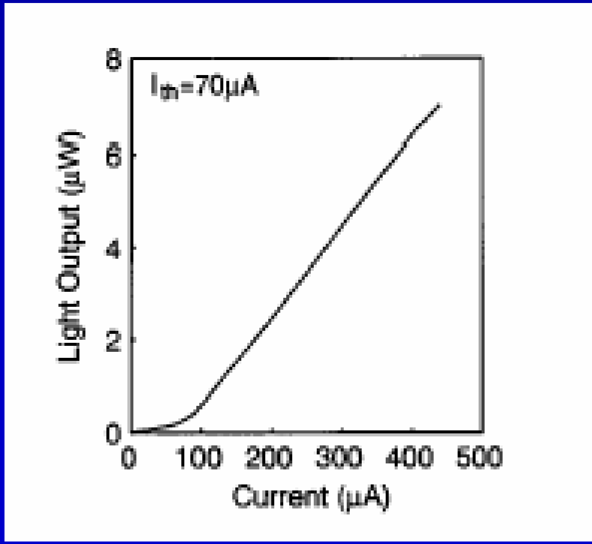
- 极低阈值电流
- 动态单模可行
- 长寿命（有源区内置）
- 容易与光纤耦合
- 可在片测试，降低成本
- 可形成高密度二维阵列



中波段：980nm

- 材料：GaInAs-GaAs
- 最近记录：阈值数十个微安，室温连续波运行
- 理论预计阈值为1微安
- 技术已较成熟：选择性氧化已成为标准光电限制结构，通过在（311）B衬底生长可避免极化不稳定。
- 可用于10Gbps LAN市场

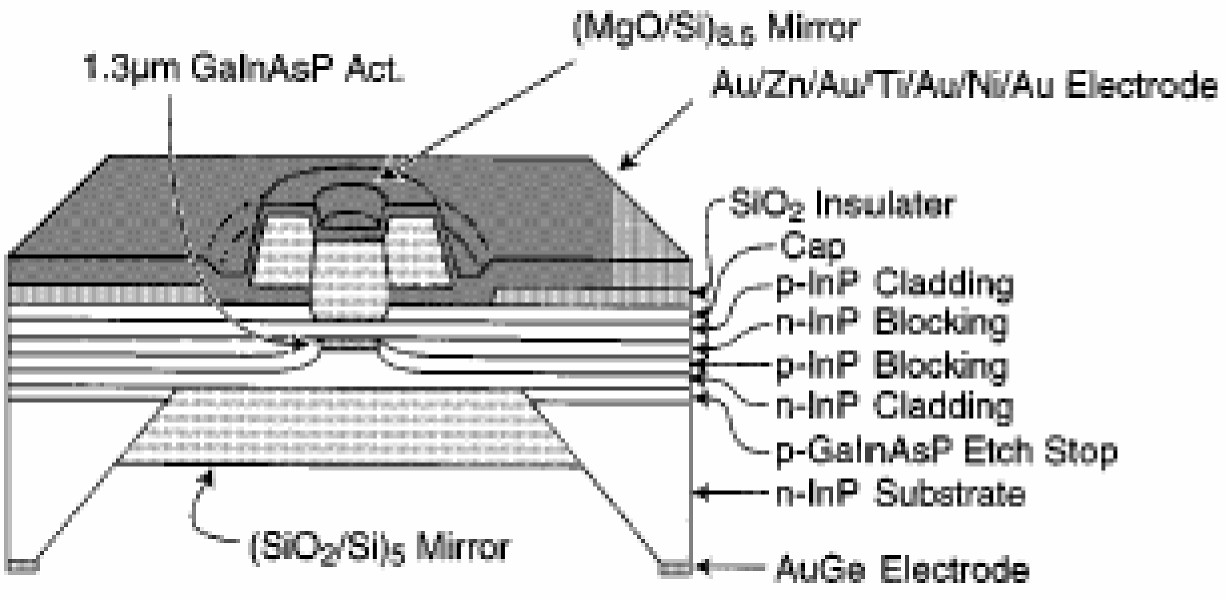




长波段： GaInAsP-InP

- 材料：GaInAsP-InP 用于干线通信（1.3um 1.5um）
- 困难：电子限制弱、Auger复合严重、 GaInAsP与InP折射率差小难以制作DBR镜面
- 解决方案：三氧化二铝和硅构成DBR、氧化镁和硅DBR，另外也可用外延键合（epitaxial bonding）方法制作有源区及GaAs-AlAs 镜面
- 上述两种方法均得到了较好结果，但第二种方法需耗费较多晶片，成本较高
- 近期研究：AlGaAsSb-GaAs构成的DBR镜面、隧道结及AlAs氧化物限制结构

1300nm VCSEL with dielectric DBR

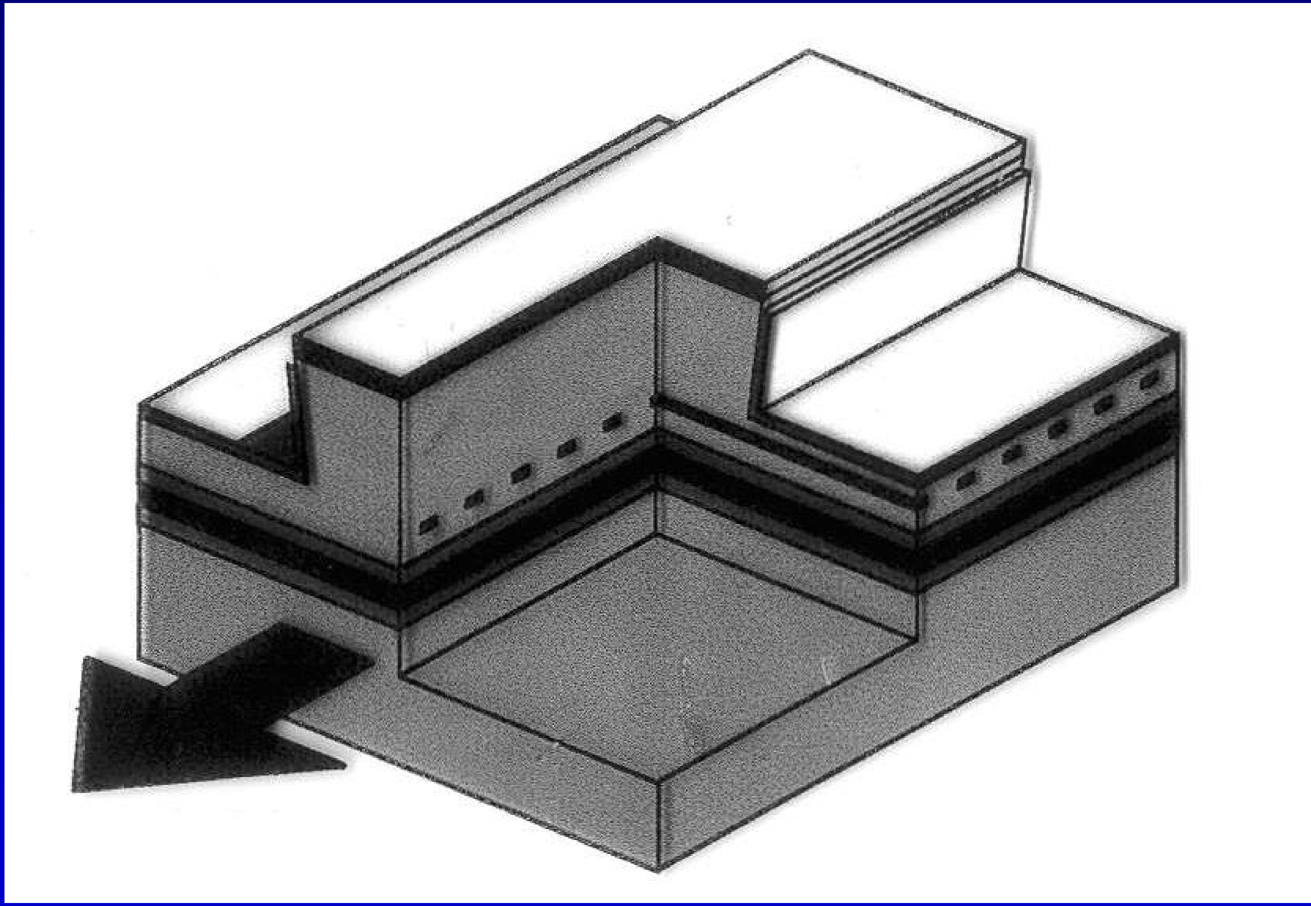


1300-nm VCSELs with thermally conductive dielectric DBR.

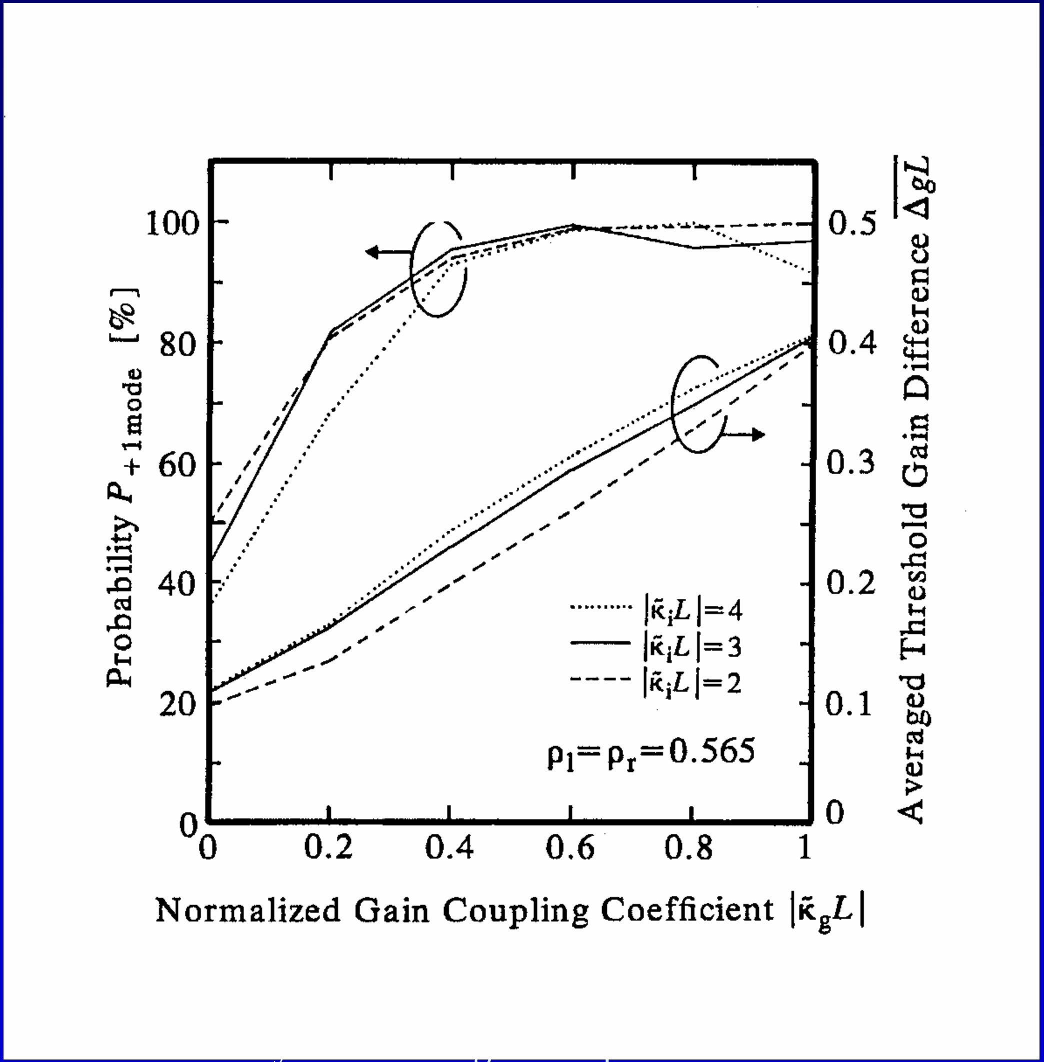
长波段： GaInNAs-GaAs

- 材料： **GaInNAs-GaAs**晶格匹配。
- 优点：如能将氮含量增加到**5**％，则**1300－1500nm**波段可被覆盖，同时**GaAs-AlAs DBR**容易制作，各种基于**GaAs**的器件结构都可用于此材料
- 此材料的使用将极大改变**VCSEL**在长波段的特性
- 目前水平：**1.3μm** 接近实用水平

增益耦合DFB-LD

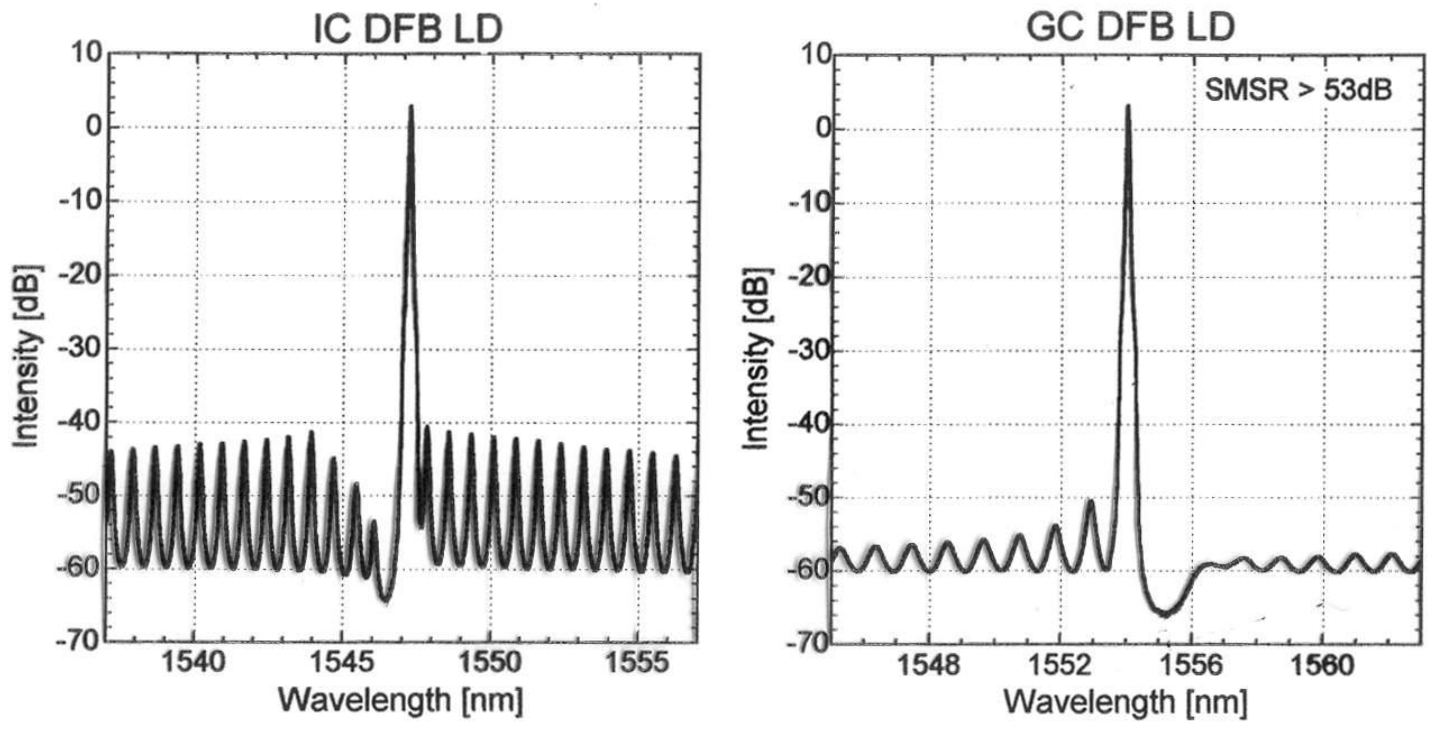


成品率的计算结果

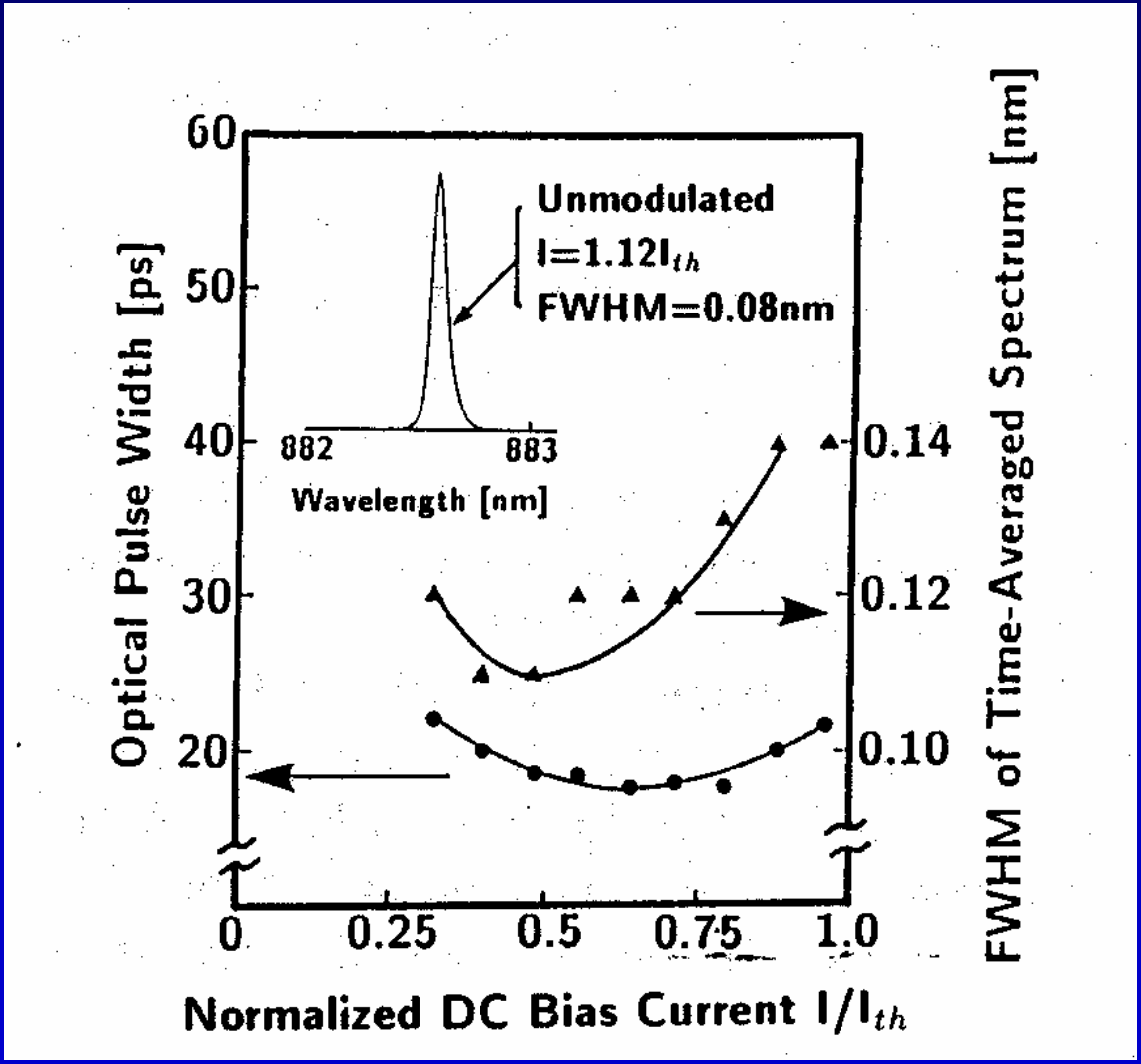


100
80
60
40
20
0
0
0.2
0.4
0.6
0.8
1
0.5
0.4
0.3
0.2
0.1
0
Probability $P_{+1\,mode}$ [%]
Averaged Threshold Gain Difference $\overline{\Delta gL}$
$|\tilde{\kappa}_i L|=4$
$|\tilde{\kappa}_i L|=3$
$|\tilde{\kappa}_i L|=2$
$\rho_l=\rho_r=0.565$
Normalized Gain Coupling Coefficient $|\tilde{\kappa}_g L|$

光谱的比较


IC DFB LD
Intensity [dB]
10
0
-10
-20
-30
-40
-50
-60
-70
1540
1545
1550
1555
Wavelength [nm]
GC DFB LD
SMSR > 53dB
Intensity [dB]
10
0
-10
-20
-30
-40
-50
-60
-70
1548
1552
1556
1560
Wavelength [nm]

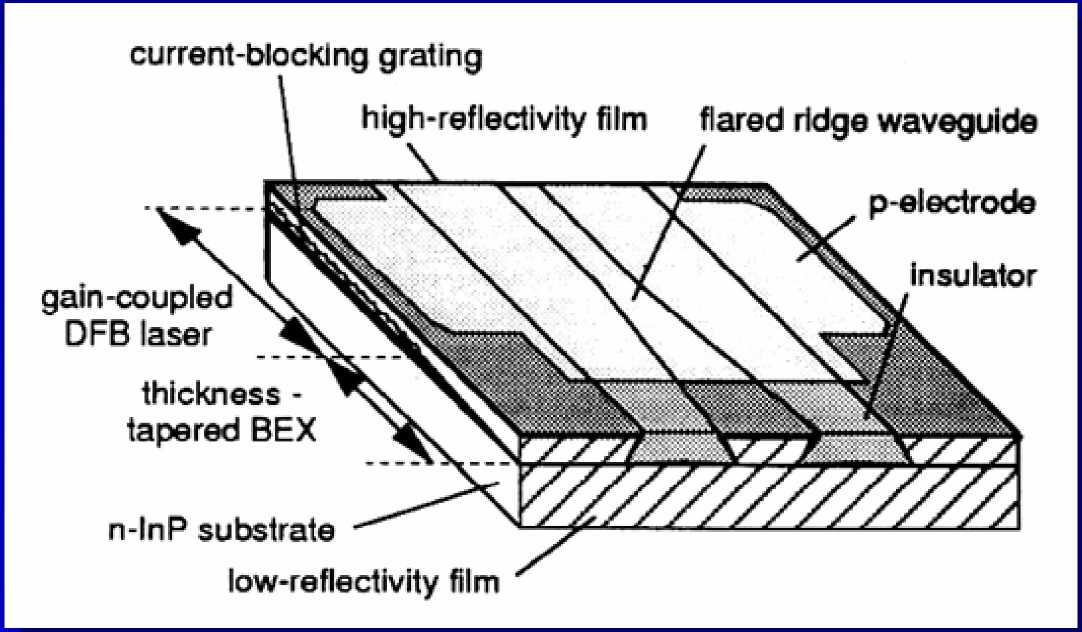
光谱与脉冲宽度的关系



Unmodulated
I=1.12I$_{th}$
FWHM=0.08nm
882
883
Wavelength [nm]
Optical Pulse Width [ps]
60
50
40
30
20
0.14
0.12
0.10
FWHM of Time-Averaged Spectrum [nm]
0
0.25
0.5
0.75
1.0
Normalized DC Bias Current I/I$_{th}$

Uncooled Gain-Coupled DFB LDs

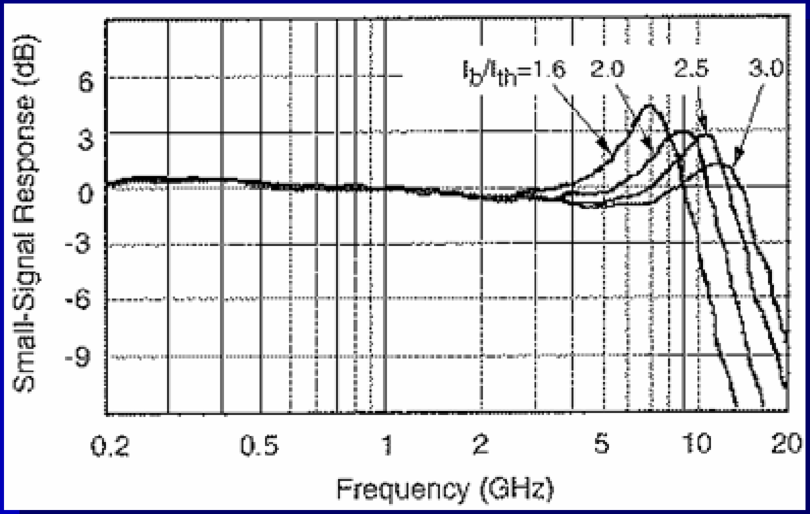
- Stable single mode operation from - 40 to 85°C
- Integrated beam-expander for improved coupling tolerance
- Gain-coupled DFB lasers with current-blocking gratings



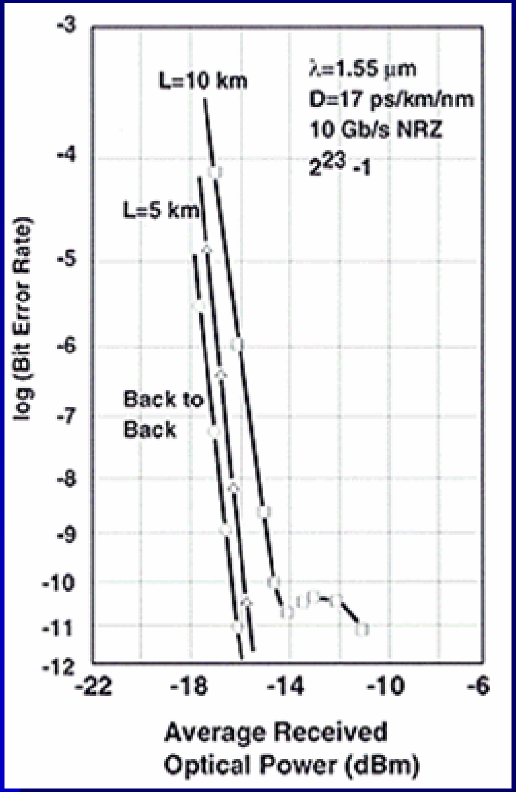
Directly Modulated DFB LDs

- *Applications*
  - Gigabit Ethernet
  - Metropolitan transmission
  - Bit rate: up to 10 Gb/s
  - Wavelength: 1.3 μm & 1.55 μm
- *Limitations*
  - Limited transmission span (< 20 km) due to large linewidth enhancement factor α (> 4)
  - Modulation speed is limited by carrier relaxation oscillation

10 Gb/s Directly Modulated DFB LDs for Metropolitan Data Transmission



Small-signal RF Response



BER Characteristics

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- Device Structures of Recent work
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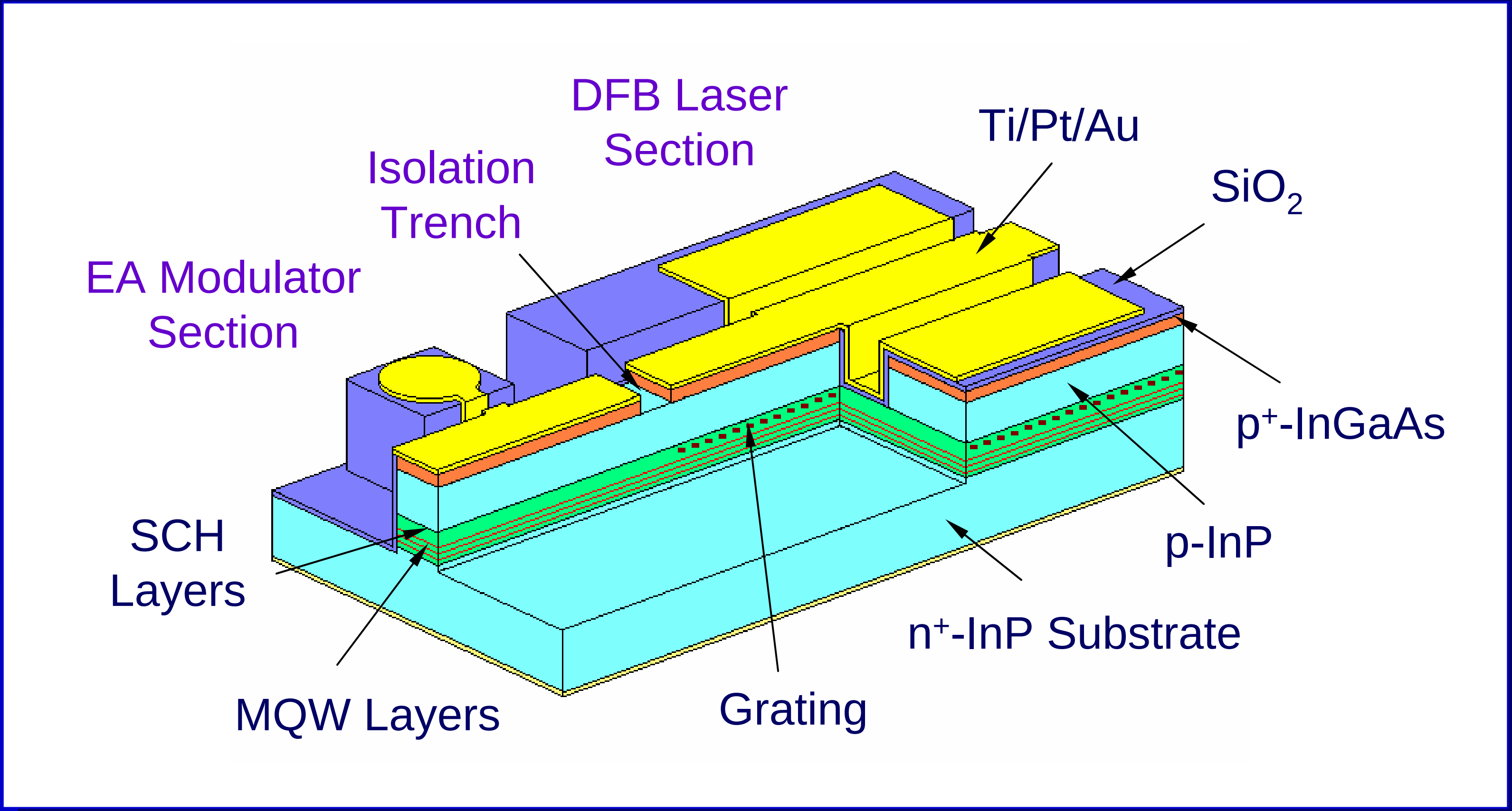
Schematic of EA Modulator Integrated DFB Laser Diode



Wavelength Compatibility in EMLs

- Wavelength Compatibility for Integrated EA
  - Lasing wavelength of the DFB laser should be on the longer wavelength side of the absorption edge of the EA modulator
- Integration Schemes
  - Butt-joint Integration
  - Selective Etching
  - Selective Area Growth
  - Quantum Well Interdiffusion

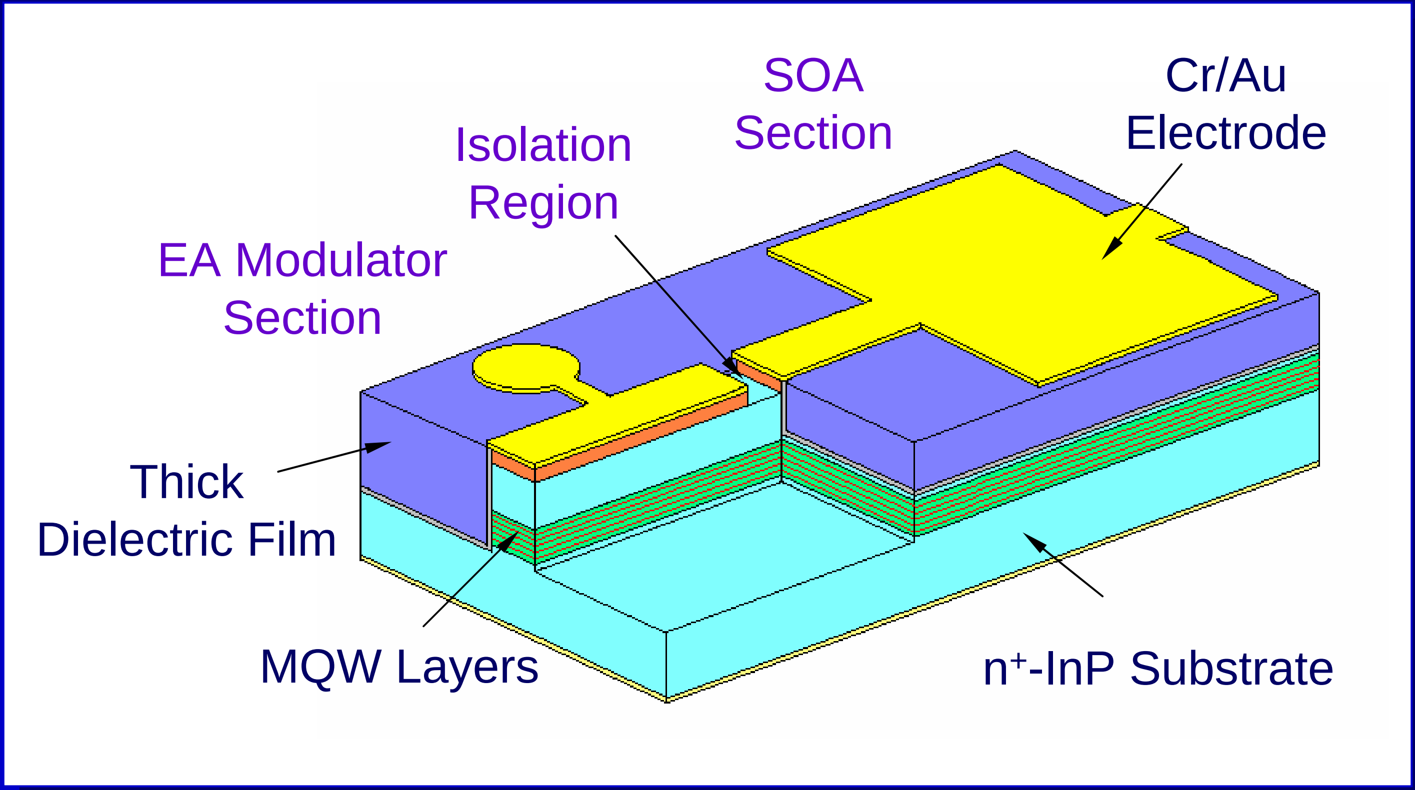
} $Eg_{Modulator} > Eg_{Laser}$

Identical Epitaxial Layer Structure $\Rightarrow \lambda_{Bragg} > \lambda_{Exciton}$

Concept of IEL Integration Scheme

- Identical Epitaxial Layer Scheme
  - Identical MQW structure for laser & modulator
  - Bragg wavelength detuned from gain peak
- What Makes IEL Feasible?
  - Wide gain spectrum of strained-layer MQW
  - Junction temperature difference between laser and modulator
  - Carrier-induced band-gap shrinkage effect
- Advantage of IEL Scheme
  - Simplified fabrication procedure $\Rightarrow$ Improved reproducibility and higher yield

IEL Structure Based SOA Integrated EA Modulator



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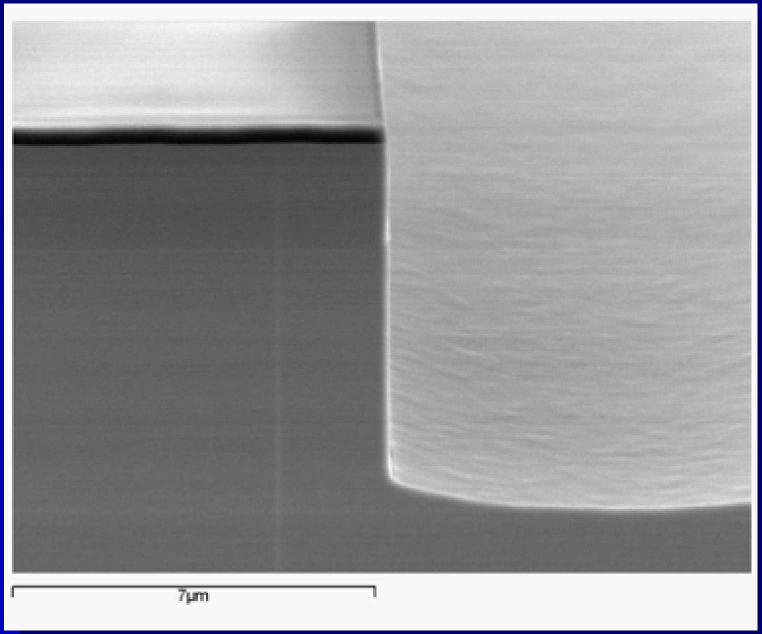
- Key Fabrication Technologies
- Characteristics
- Fabrication and Characteristics of Module for 40 Gb/s Applications

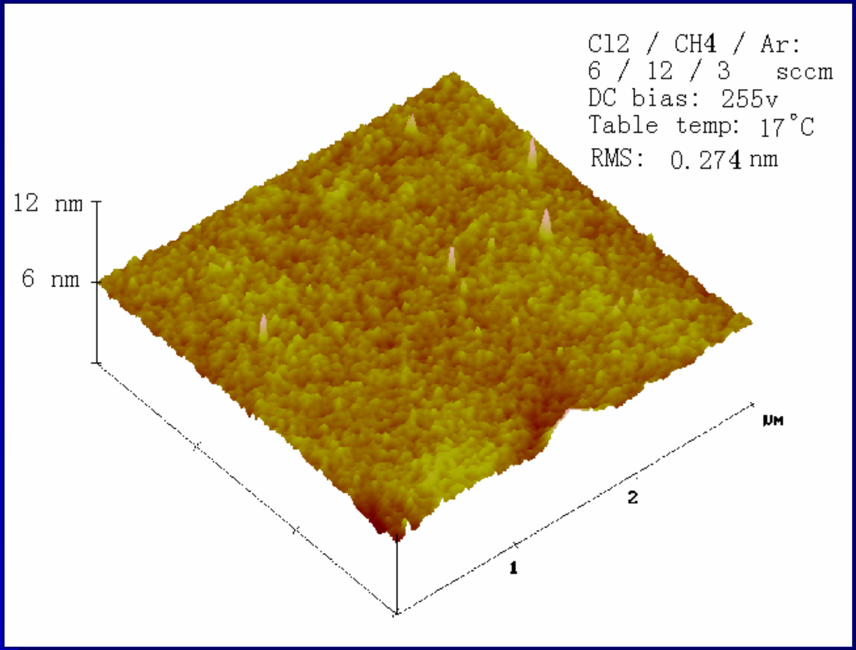
ICP Dry Etching for InGaAsP/InP Integrated Devices

- Advantages of Dry Etching Technology
  - High anisotropy & resolution
  - Good reproducibility & dimensional control
- Inductively Coupled Plasma Dry Etching
  - High plasma intensity $\Rightarrow$ High etch rate
  - Low bias $\Rightarrow$ Low damage
  - Better controllability & Lower cost
- $Cl_2/CH_4/Ar$ ICP Etching for EML Fabrication
  - Vertical sidewall & Smooth surface
  - Precise control of ridge width in EA section

Dry Etching of InP-Based Semiconductors by ICP



SEM Image of Etched Sidewall



Surface Morphology Measured by AFM
(RMS Roughness: 0.27 nm)

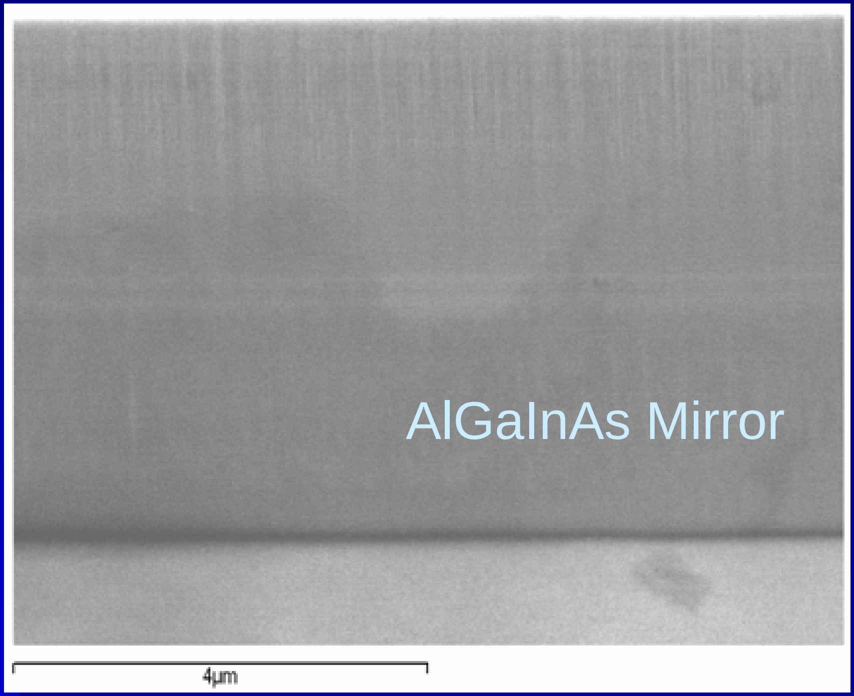
ICP Dry Etching for AlGaInAs/InP Integrated Devices

- Difficulty in Dry-Etching of AlGaInAs
  - Oxidization of Al
  - Self-masking due to low volatility of $InCl_x$
- Dry-Etching of AlGaInAs by $Cl_2/BCl_3/CH_4$ ICP
  - BCl_3 for oxygen removal
  - CH_4 to form volatile $In(CH_3)_x$
  - Cl_2 for increased etch rate

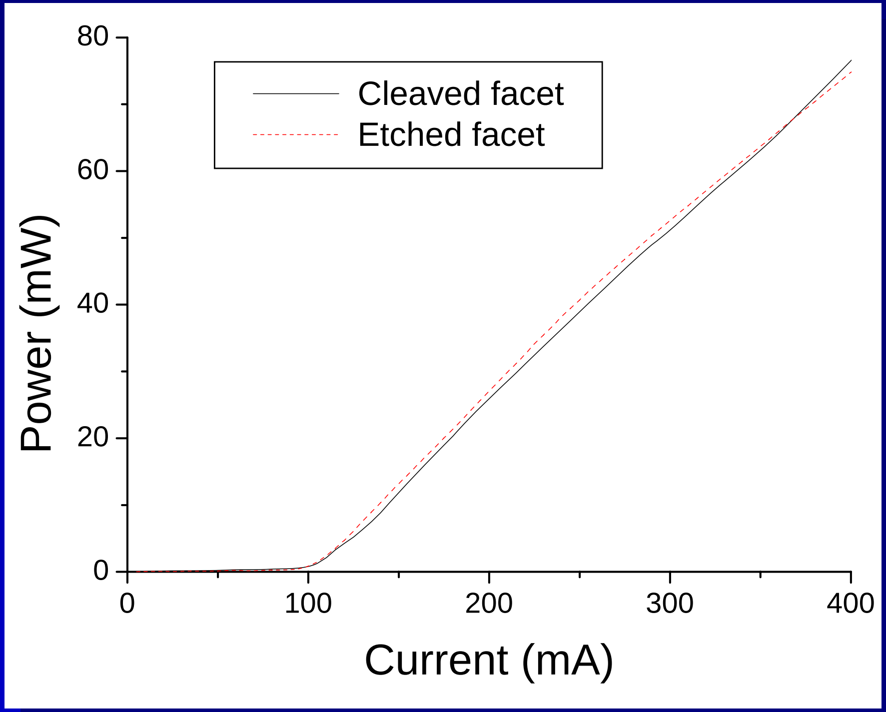
AlGaInAs MQW Laser Diodes with Etched Facets

- Why AlGaInAs MQWs?
  - Larger conduction band discontinuity
    - $\Delta E_c/\Delta E_g \sim 0.7$
  - Better thermal behavior
    - $T_c \sim 120$ K
- Why Etched Facets?
  - Laser cavity formed without cleaving into bar
  - On wafer test made possible

Performance of Etched-Facet AlGaInAs MQW Lasers



AlGaInAs Mirror Etched by $Cl_2/BCl_3/CH_4$ ICP

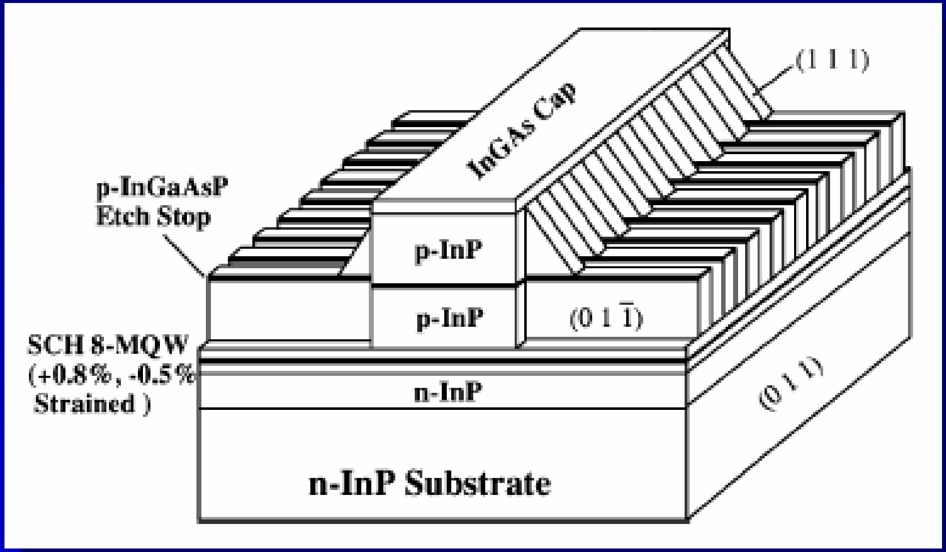


I-L Curves of Lasers with Cleaved & Etched Facets

Regrowth-Free DFB Lasers

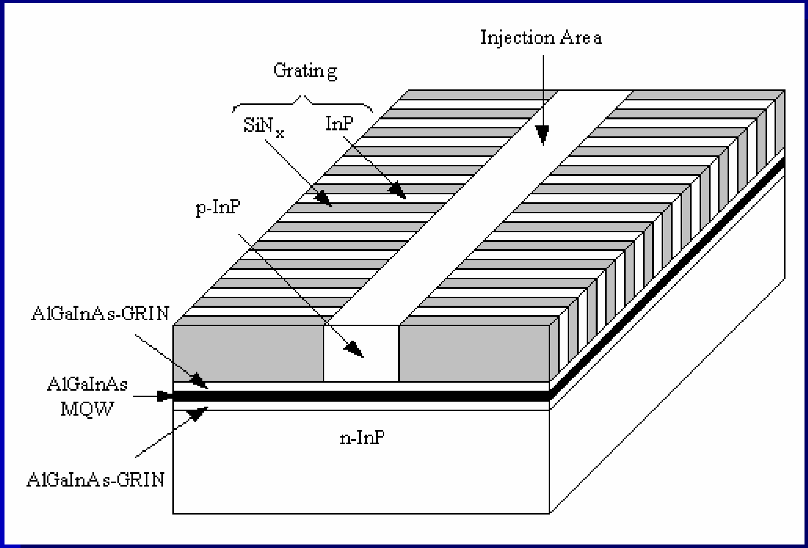
- Conventional DFB Lasers
  - Distributed feedback by embedded gratings
  - Regrowth required after grating definition
- Lateral Coupled DFB Lasers
  - Longitudinal feedback by periodically perturbation in the lateral evanescent field
    - Deeply etched surface gratings
  - No regrowth involved

Implementation of Lateral Optical Confinement



Ridge defined before etching of gratings to provide lateral optical confinement

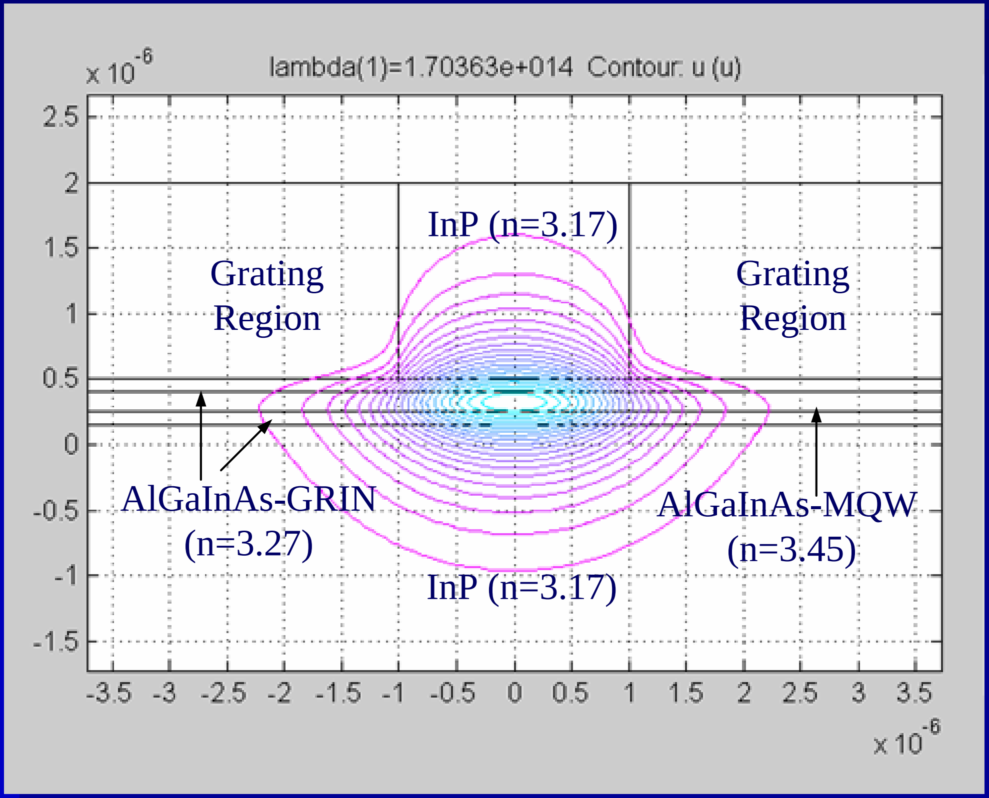
By other group



Lateral mode confinement provided by effective ridge waveguide

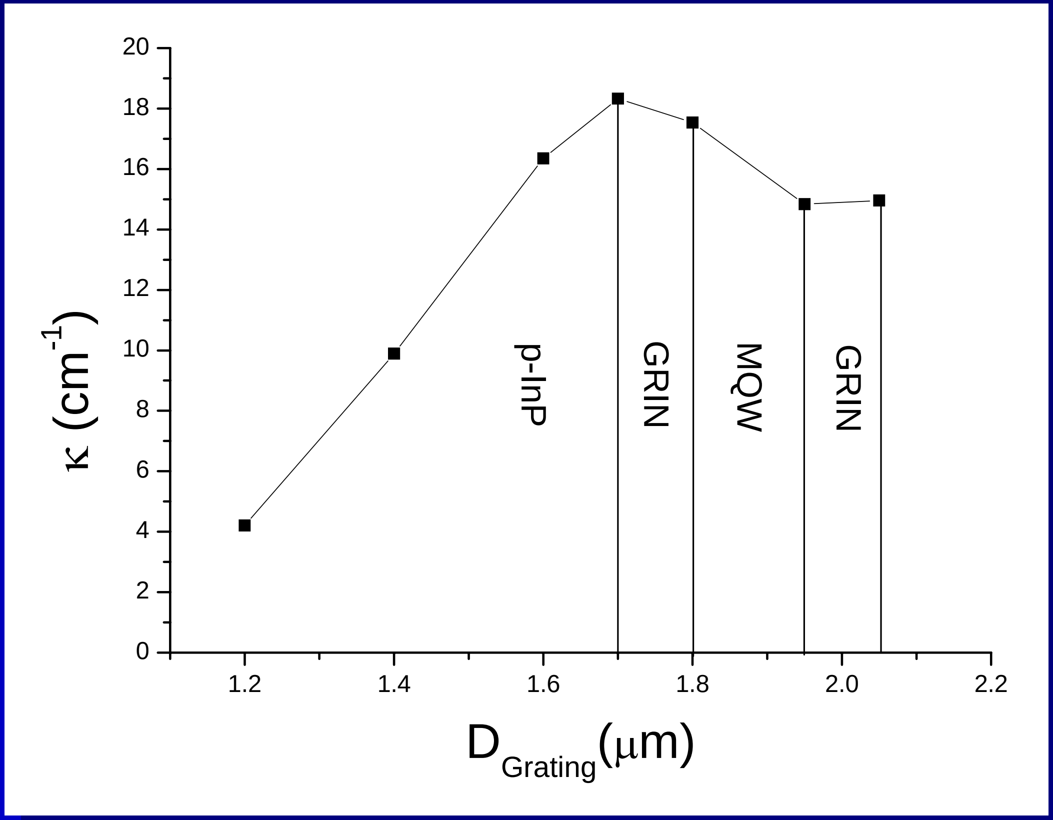
By our group

Mode Profile of Lateral-Coupled DFB Laser



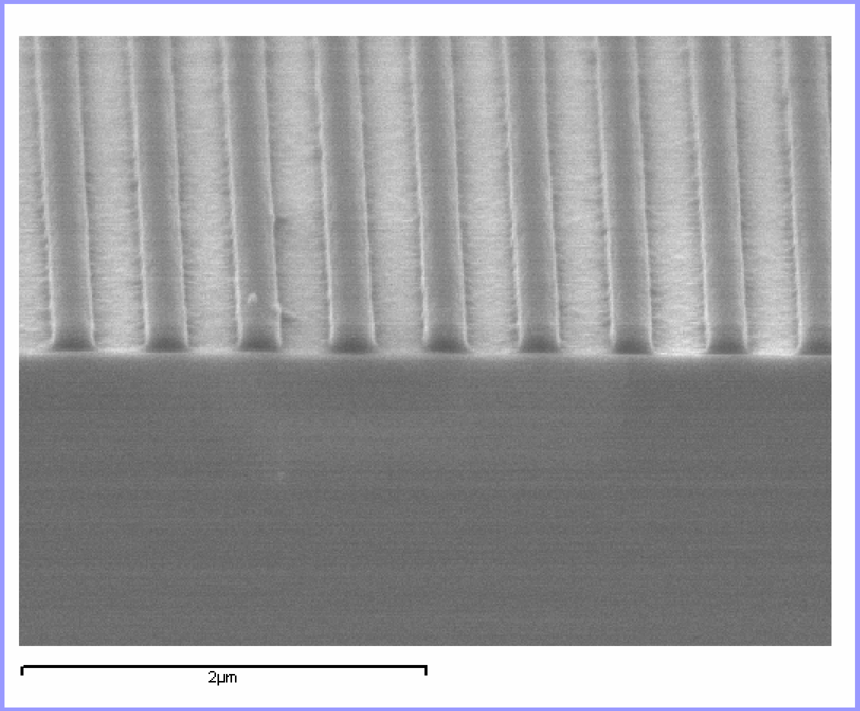
Fundamental Mode Calculated by FEM

Influence of Grating Depth on Coupling Strength

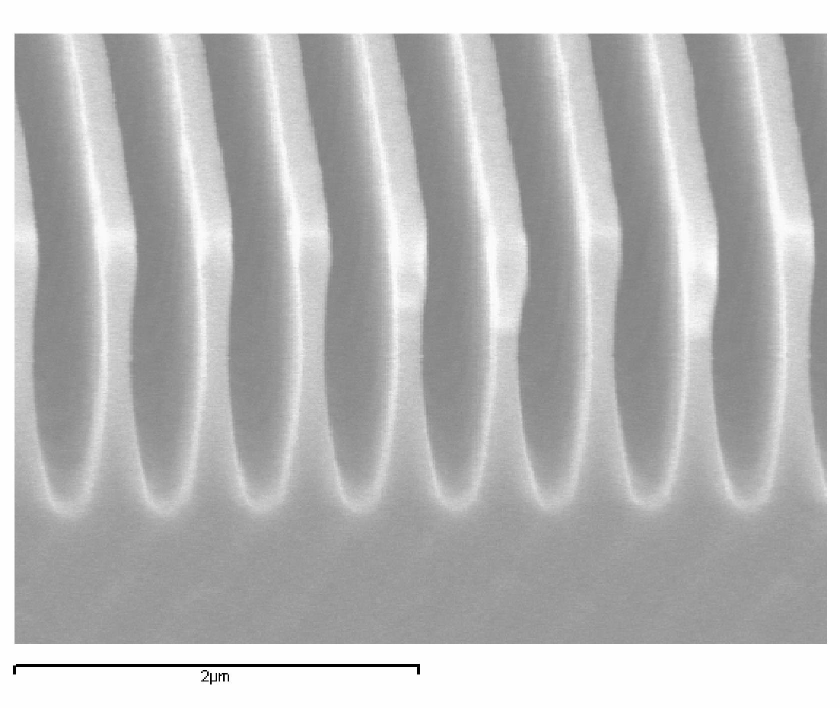


Coupling Strength vs. Grating Depth

Deep Surface Gratings Fabricated by ICP Dry-Etching

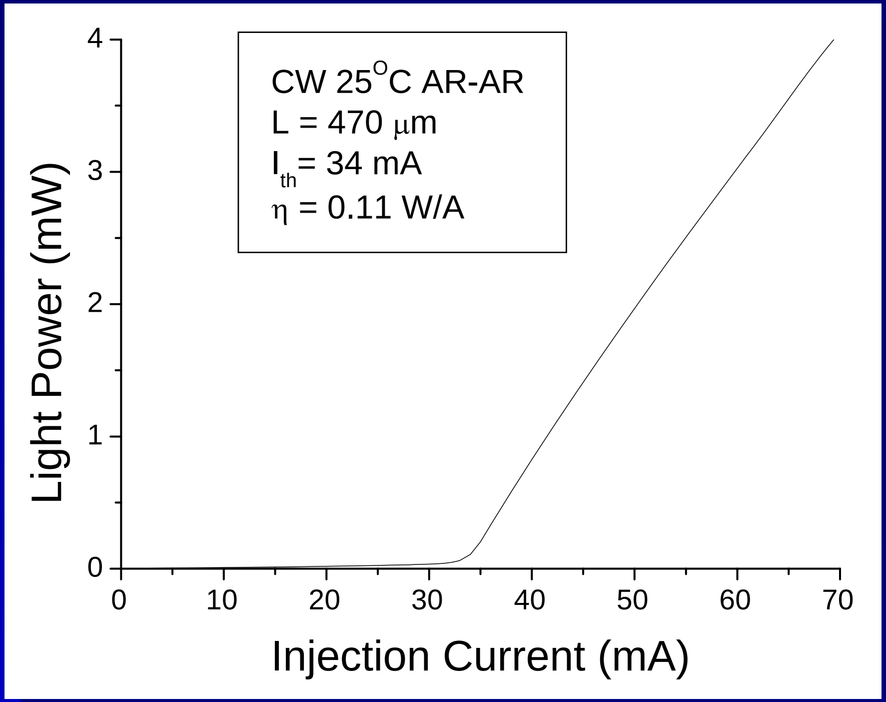


SiN_x Mask Etched with SF_6

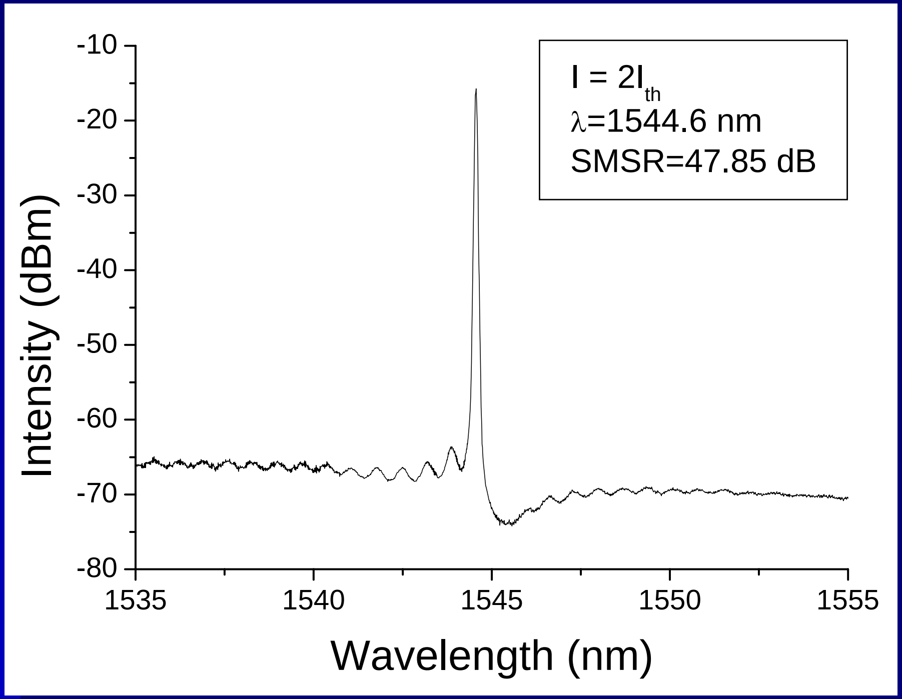


Second-Order Surface Gratings Etched by $Cl_2/CH_4/Ar$ ICP

Lasing Behavior of Lateral-Coupled DFB Laser



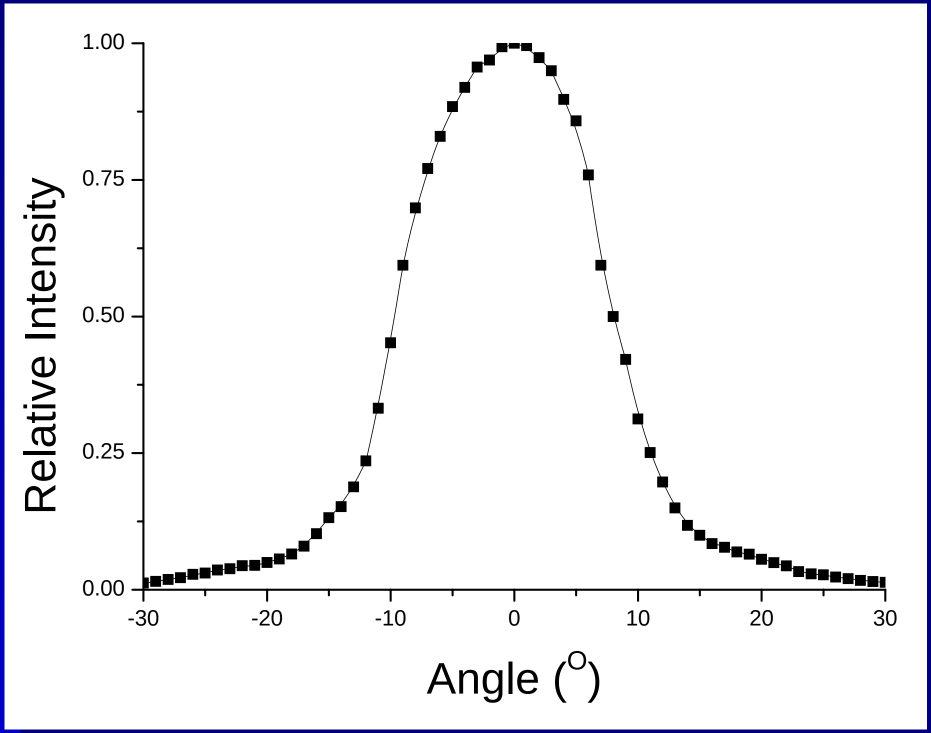
I-L Curve



Lasing Spectrum
(SMSR > 45 dB)

Wang J, Tian J B, et al. IEEE Photon. Technol. Lett., 2005, 17(7):1372-1374

Far Field Pattern Along Junction Plane

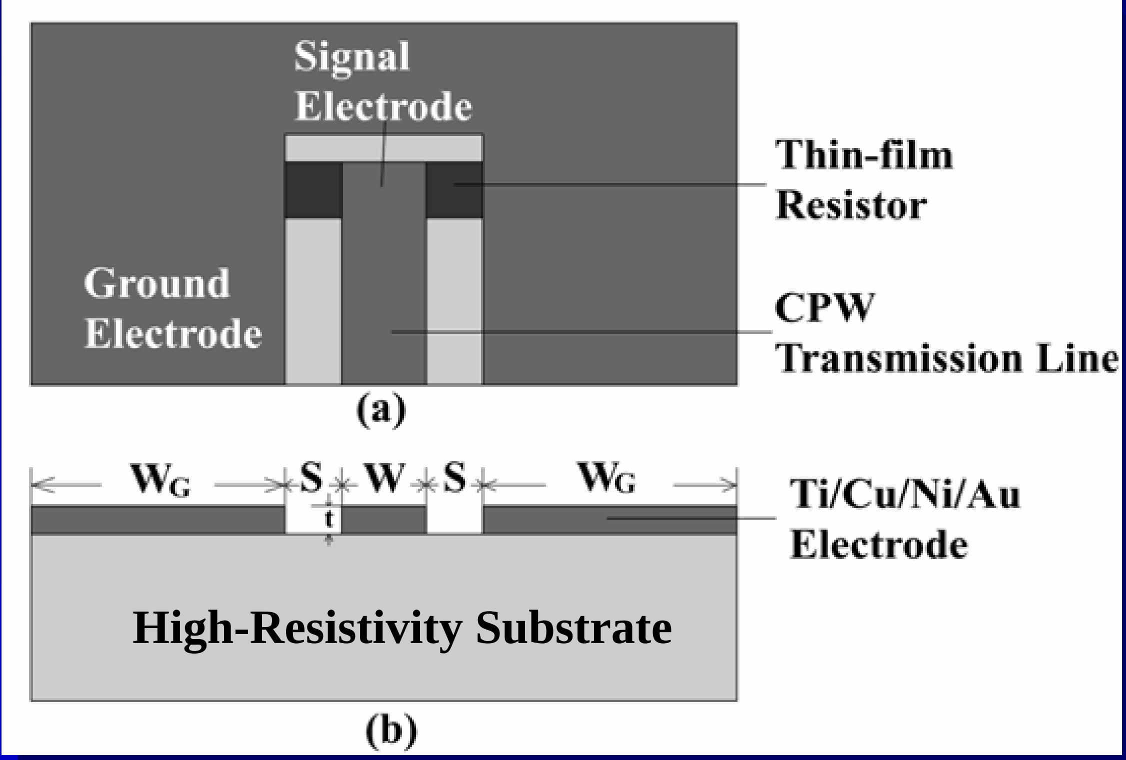


Only Fundamental Lateral Mode Observed

Submount for High-Speed EA Modulators

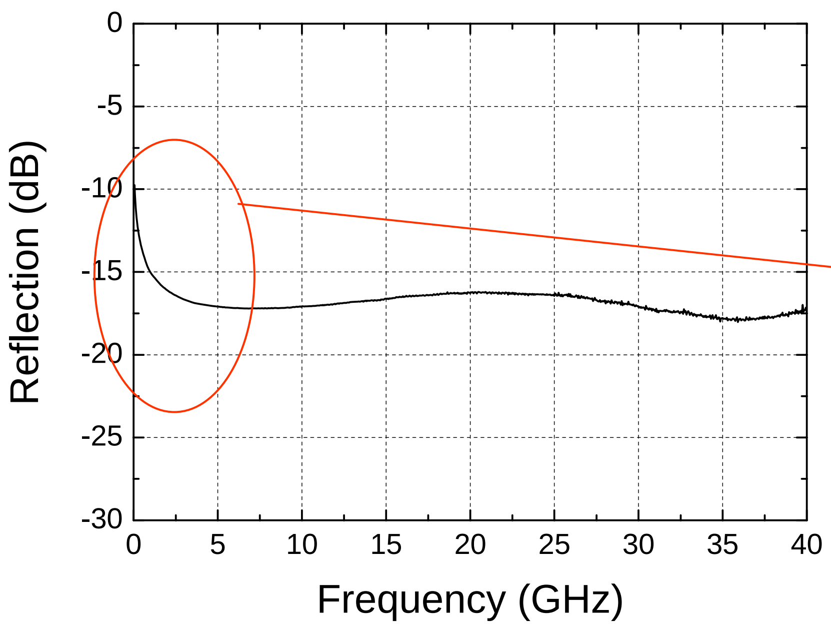
- Heat Dissipation
  - Substrate with high thermal conductance
- Modulation Signal Feeding
  - Transmission line for microwave signal feeding
  - High resistive substrate to reduce microwave loss
- Impedance Matching for EA Modulator
  - EA modulator behaves as capacitor at high frequency
  - 50 Ω sheet resistor required to reduce microwave reflection

Schematic of Submount for High-Speed EA Modulators

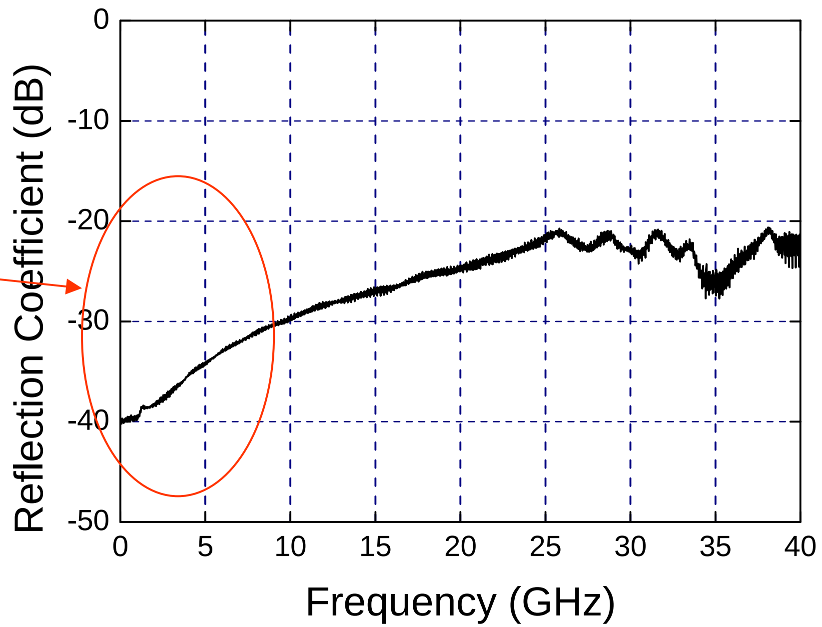


(a) Top View (b) Cross-Section View

Improved Microwave Characteristics by Use of Ti/Cu/Ni/Au Instead of Cr/Au

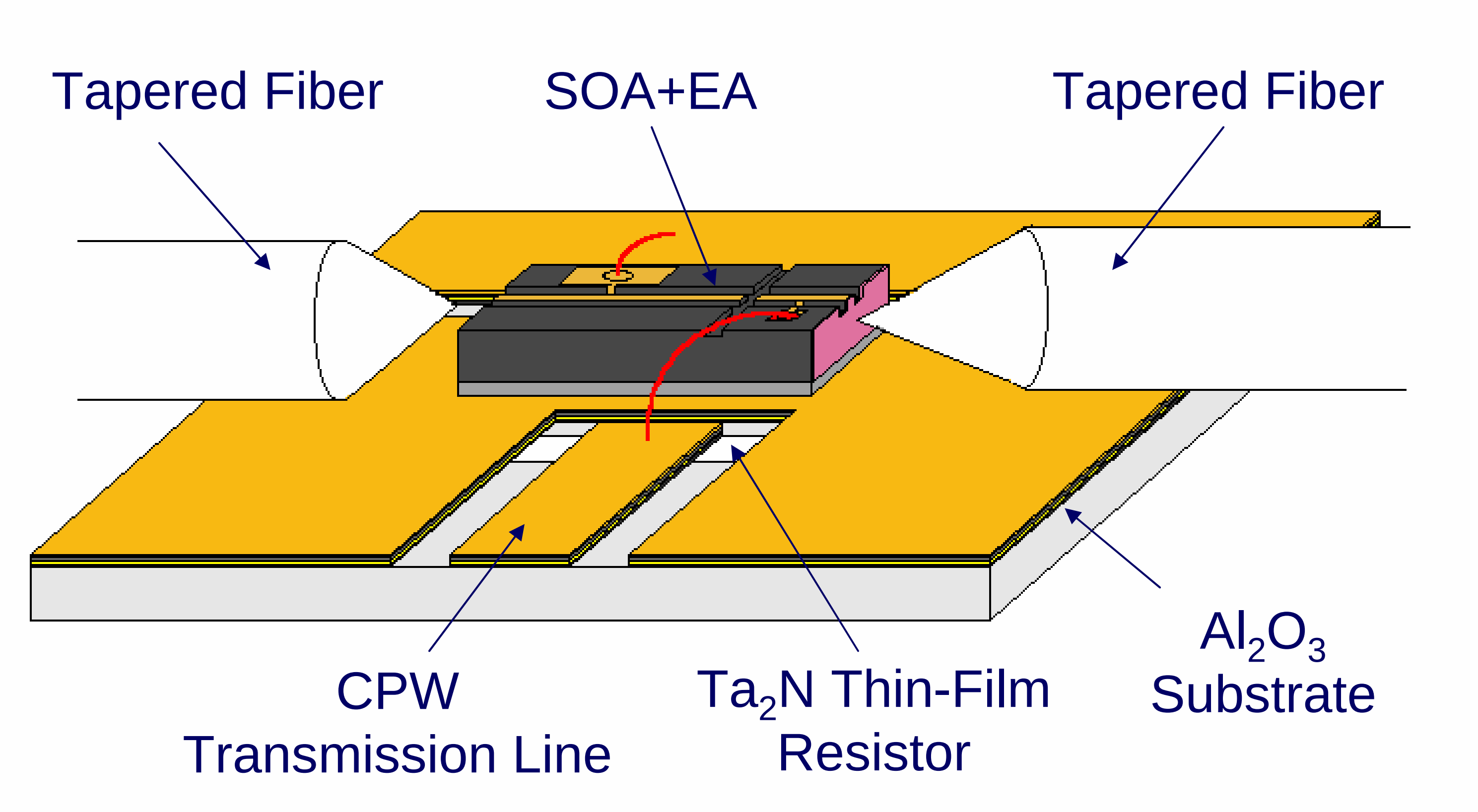


Microwave Reflection of Al_2O_3 Submount with Cr/Au Electrode



Microwave Reflection of Al_2O_3 Submount with Ti/Cu/Ni/Au Electrode

Chip-Level Packaging of EA Modulator



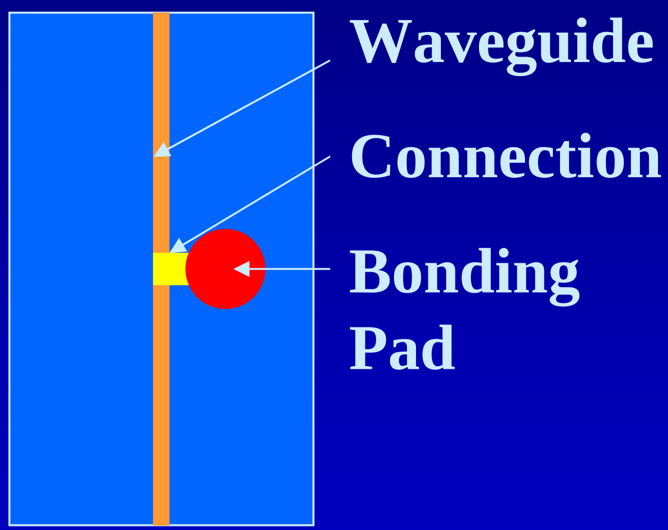
Fabrication of the Planar Electrode Structure for 40 Gb/s EA Modulator Integrated Devices

40 Gb/s EA Modulator Integrated with SOA

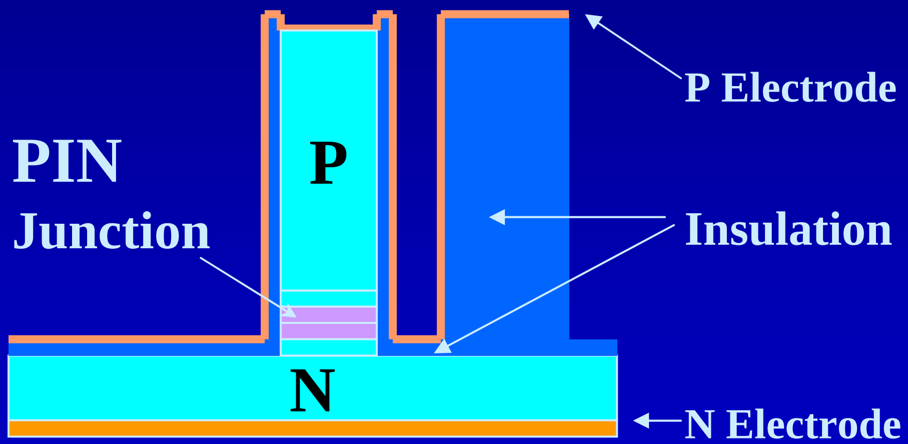
- EA Modulator Integrated with SOA
  - Compensate both coupling and absorption losses
  - IEL integration scheme adopted
- Extended Modulation Bandwidth
  - Reducing junction capacitance
    - Narrow high-mesa ridge waveguide
  - Reducing electrode capacitance
    - Thick dielectric film beneath bonding pad
  - Reducing packaging induced parasitic
    - Specially designed submount

Device Structure and Capacitance of EA Modulator

Modulator Capacitance including Junction Capacitance and Electrode Capacitance



Top View



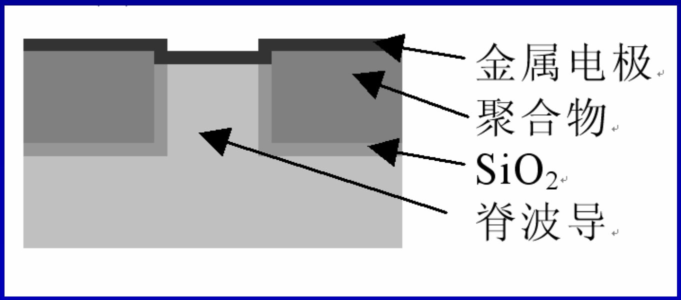
Cross-sectional View

Difficulties to Reduce Device Capacitance Further for 40 Gb/s Modulation

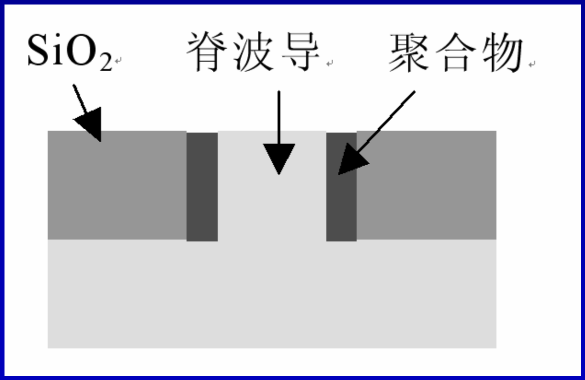
- Increase thickness of insulation film to reduce electrode capacitance, trade-off between:
  - Deep groove formed between ridge and electrode platform
  - Thickness of sidewall electrode reduced and the stability of metal connection influenced
  - Series resistance increased
- Reduce junction width to reduce junction capacitance further
  - Ridge waveguide is easier to be damaged in processes
  - Series resistance increased

Electrode Planation to Reduce Electrode Capacitance

Merit: uniform thicker electrode film, increased stability, reduced series resistance



Polyimide based Planation



Thick SiO_2 and Polymer based Planation

Air-Bridge Structure

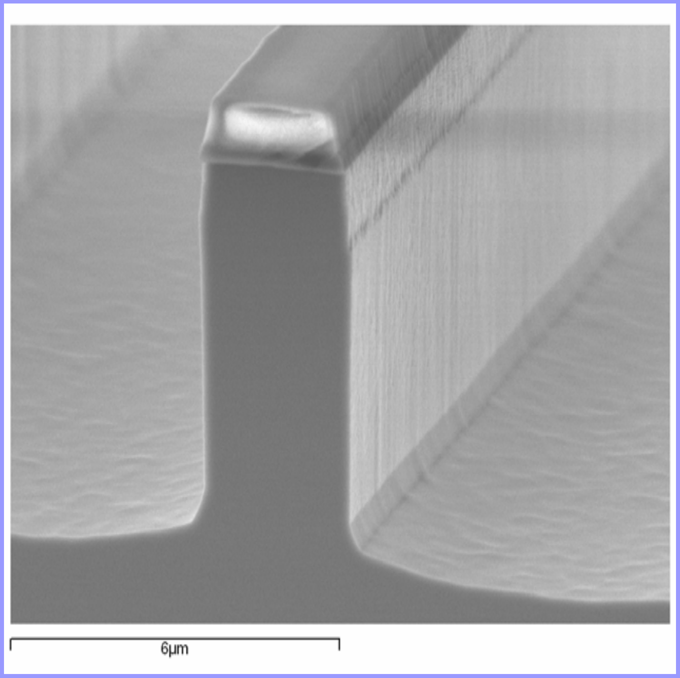
Our Choice of the Electrode Planation Technique

- Using Polyimide
  - Comparably softer to cause electrode bonding problem
  - Not well sticks to wafer and often shrinks
- By Air-Bridge Structure
  - Complex and difficult fabrication process
  - Lack of protection for bridge waveguide
- ✓ Self-developed Thick-SiO_2 based Planation Process
  - ✓ Well stick to wafer and small strain
  - ✓ Hard SiO_2 , better for electrode bonding

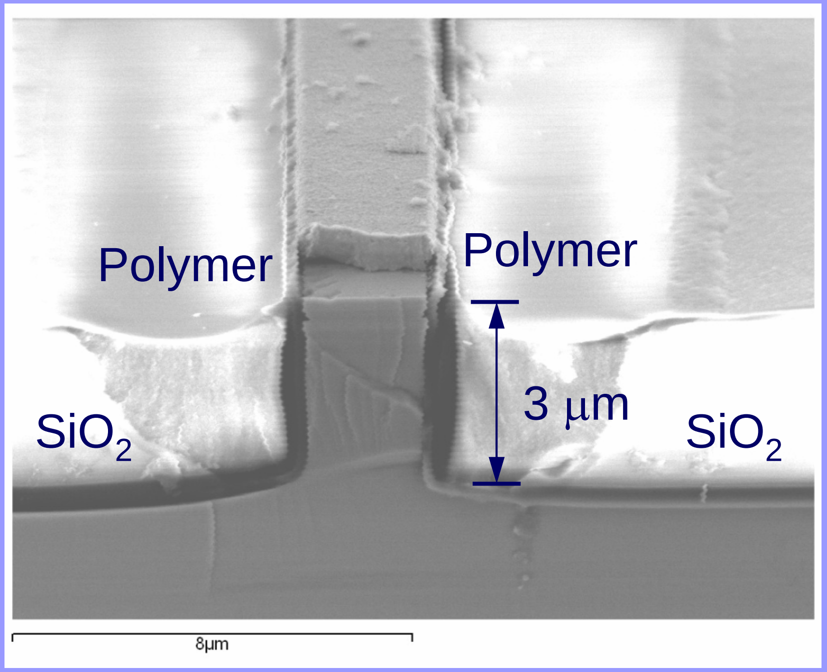
Our Choice of Reducing Junction Width

- ✓ Dry-etched High Mesa Structure：
  - Higher etched depth to benefit reducing capacitance
  - Shortcoming: lower mechanic strength of ridge waveguide
- ✓ Special shallow structure: Electric Field Confinement by etching p-layer outside ridge waveguide stripe
  - Suitable to adopt reversed ridge structure to realize wider top width, and lower contact resistance
  - Shortcoming: etching depth restricted, and insulation thickness and electrode capacitance limited

High-Mesa Ridge Waveguide

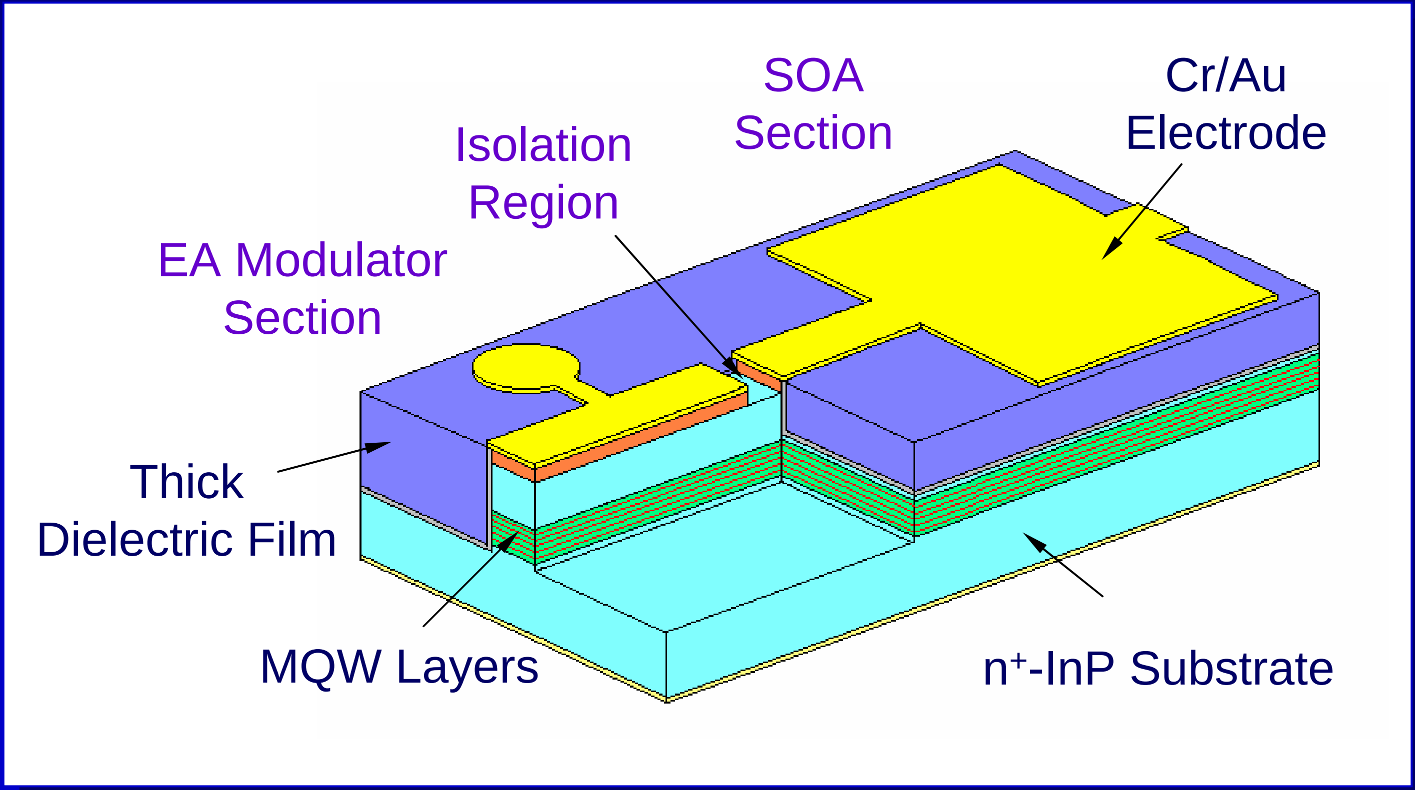


ICP Etched Narrow High-Mesa RWG Structure

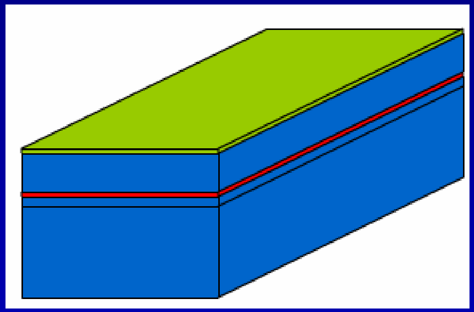


Thick Dielectric Film Below Electrode Pad

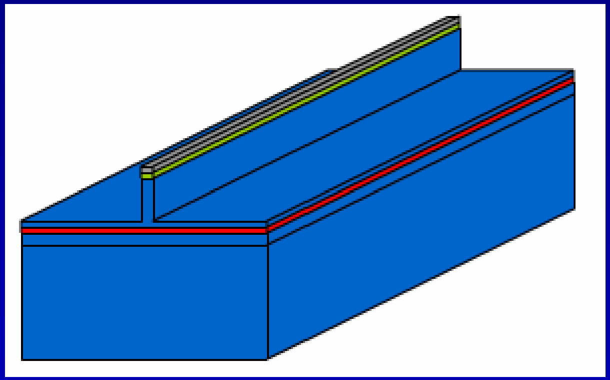
IEL Structure Based SOA Integrated EA Modulator



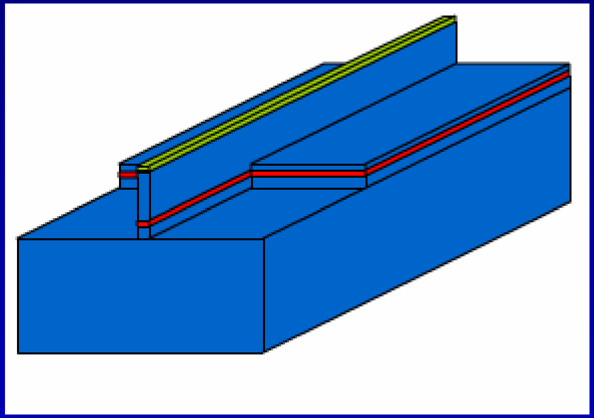
Fabrication Processes of Identical Epitaxial Layer Structure Based SOA/EA Modulator Integrated Devices (1)



Epitaxial Growth of Device Material

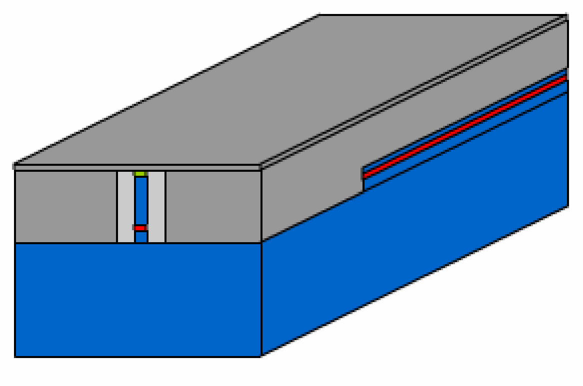


2 μm-wide Wet Etched Ridge Waveguide in Both Sections

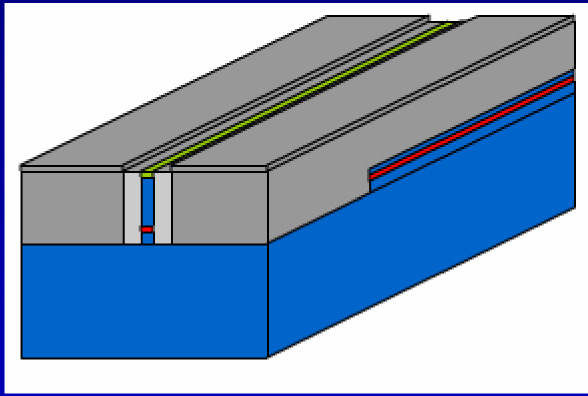


ICP Dry-Etched 4 μm-high Ridge Waveguide in EA Modulator

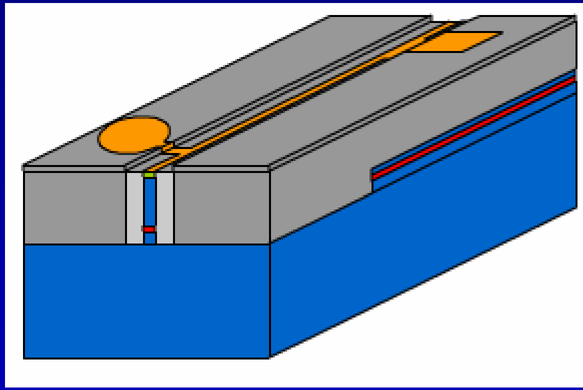
Fabrication Processes of Identical Epitaxial Layer Structure Based SOA/EA Modulator Integrated Devices (2)



Thick SiO_2 and Polymer based Insulation Planation

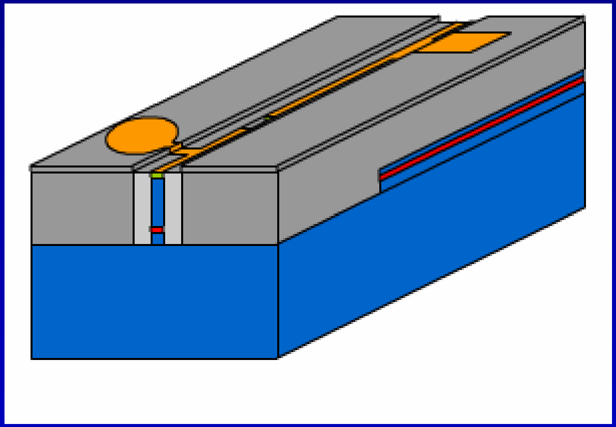


Uncovering Electrode Window

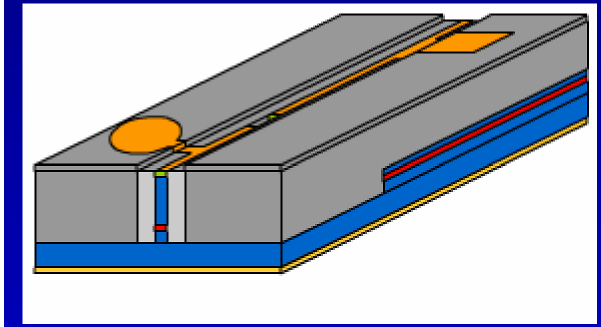


Forming Cr/Au Patterned P-Side Electrode

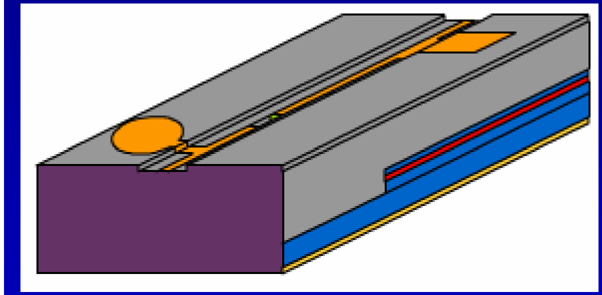
Fabrication Processes of Identical Epitaxial Layer Structure Based SOA/EA Modulator Integrated Devices (3)



Electrode Isolation between SOA and EA Modulator



Backside Thinning and Deposition of N-type Electrode

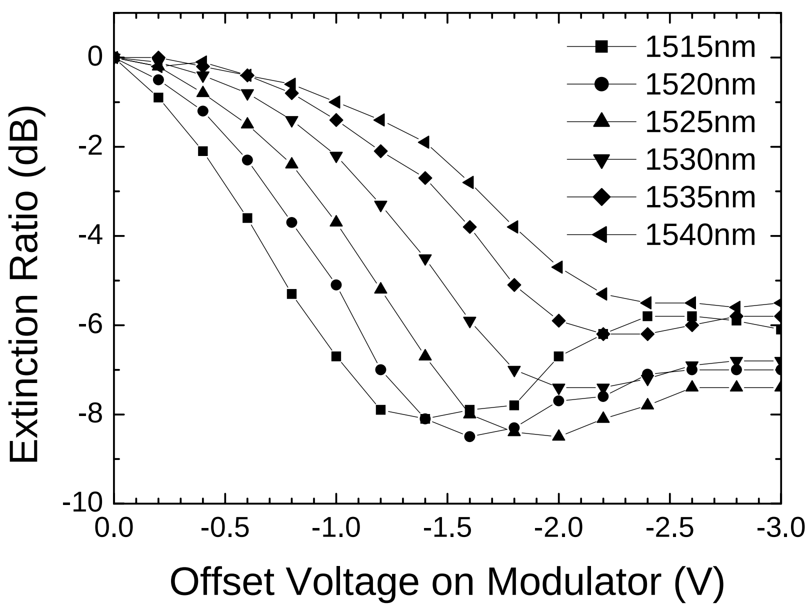


Cleaving Chip and AR Coating at Both Facets

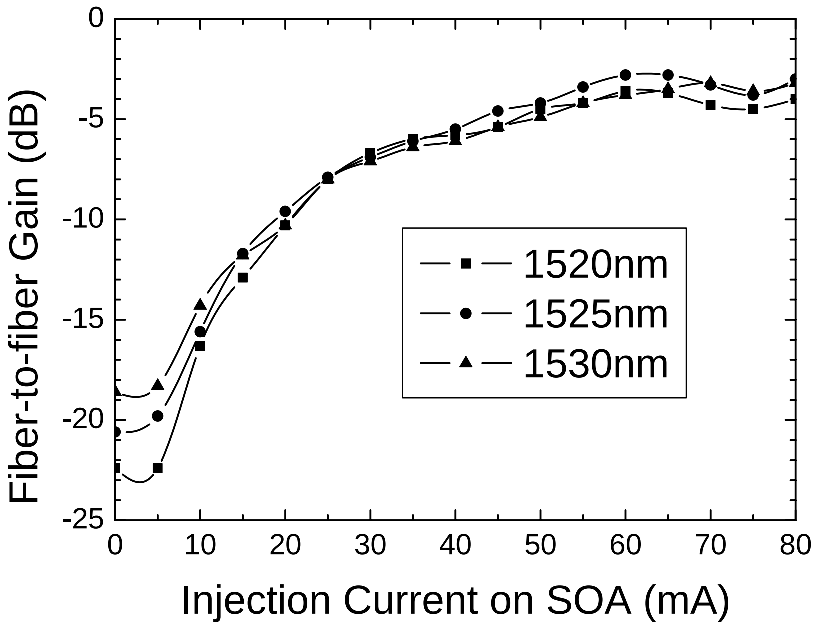
Outline

- Brief Introduction
- Device Structure of Recent Work
- Fabrication Technologies
- Characteristics
- Fabrication and Characteristics of Module for 40 Gb/s Applications

Static Characteristics of Integrated SOA/EA Modulator

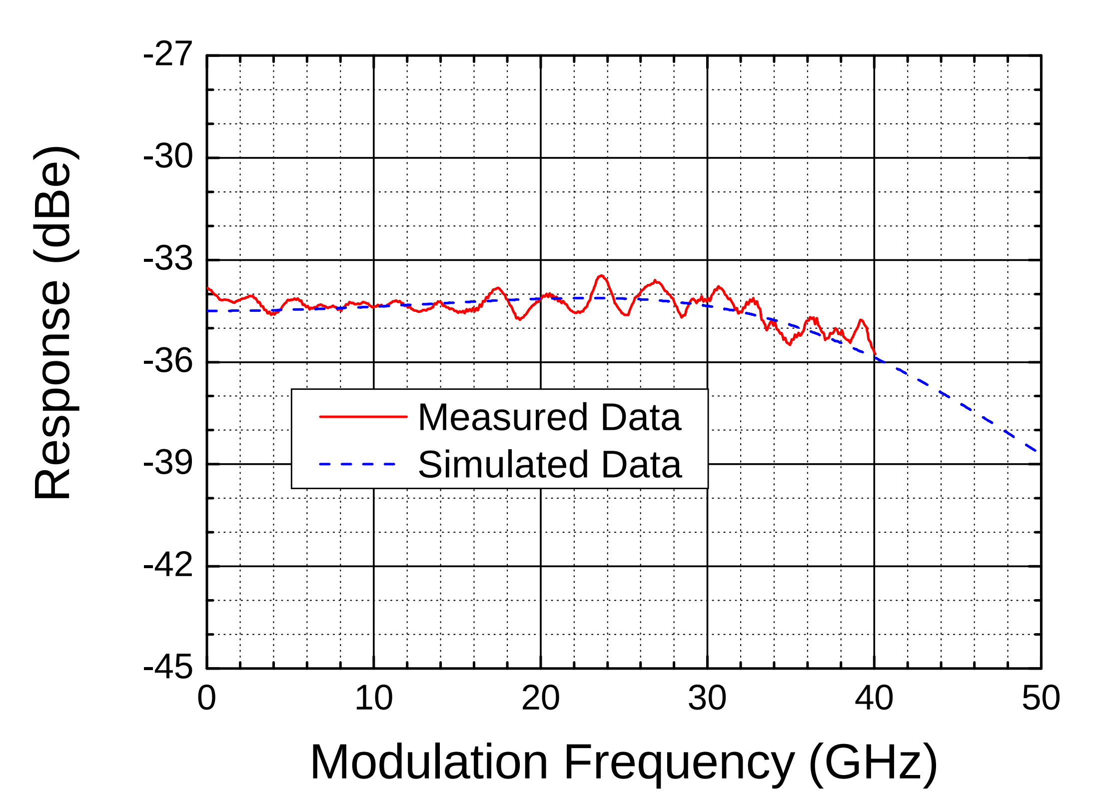


Extinction Ratios of Integrated EA Modulator



Amplification Performance of SOA

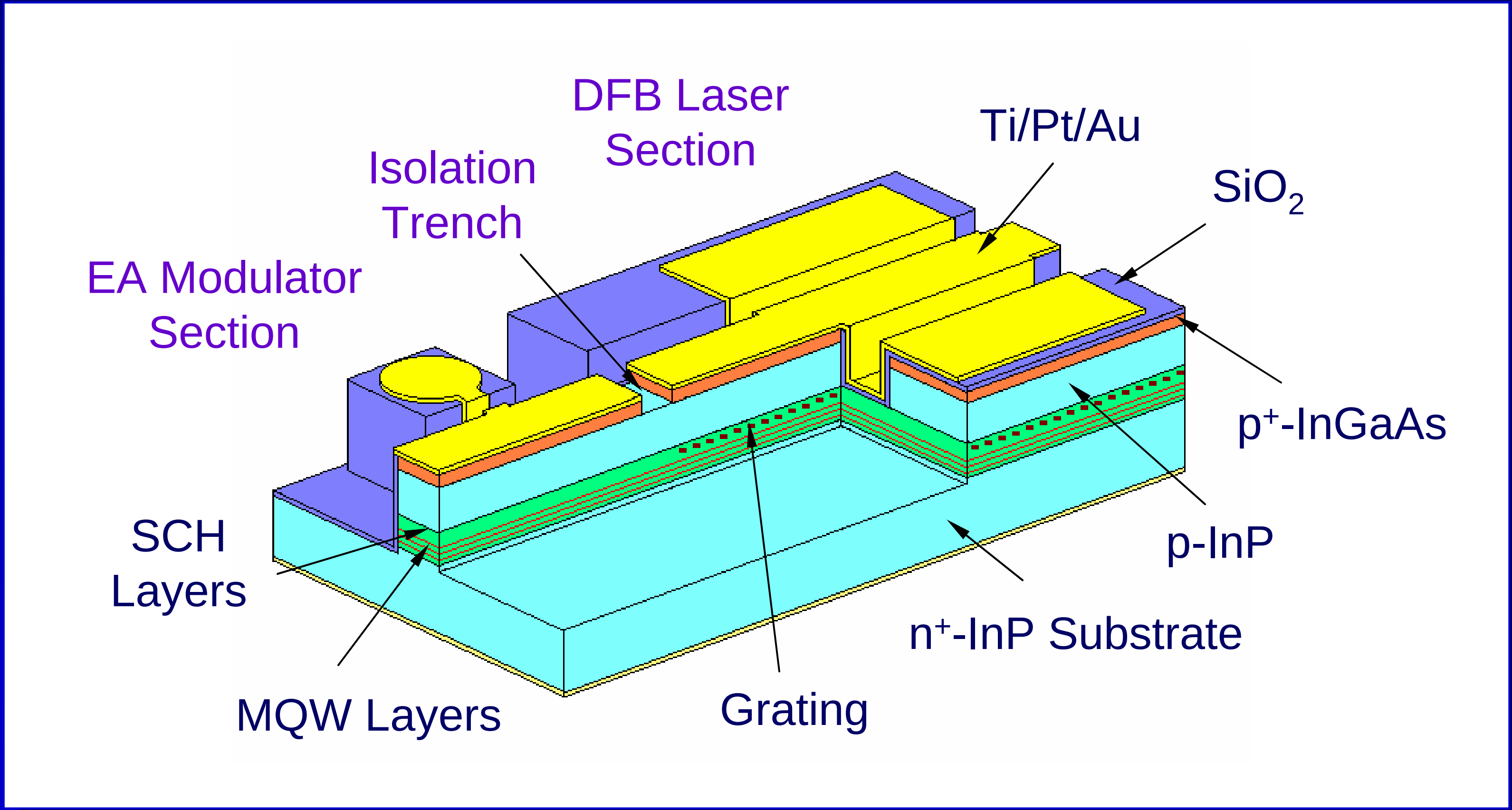
Integrated Device for 40 Gb/s System



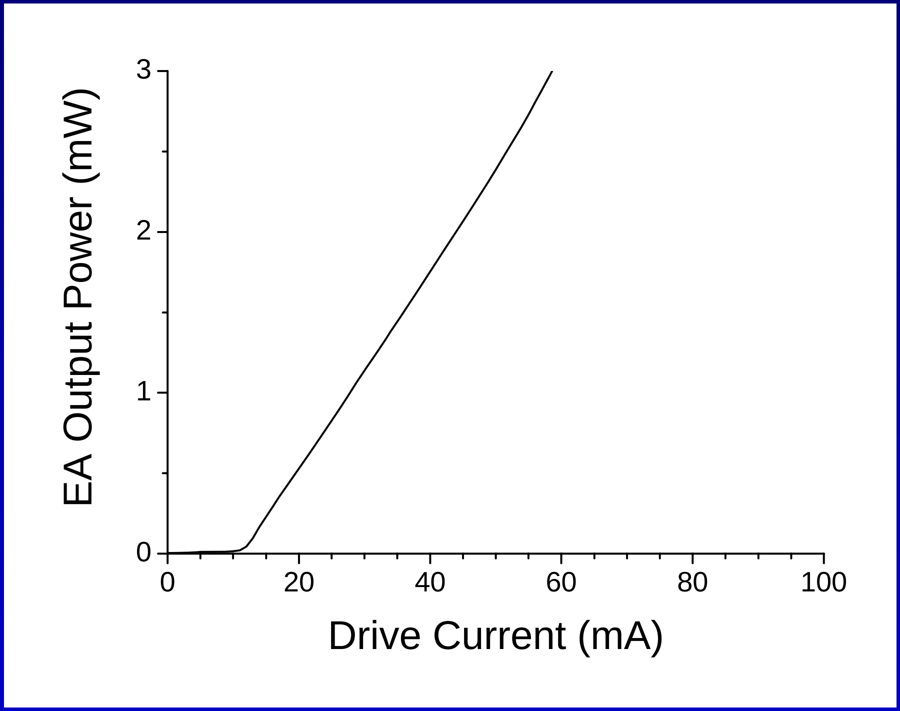
BW (3 dBe) > 40 GHz

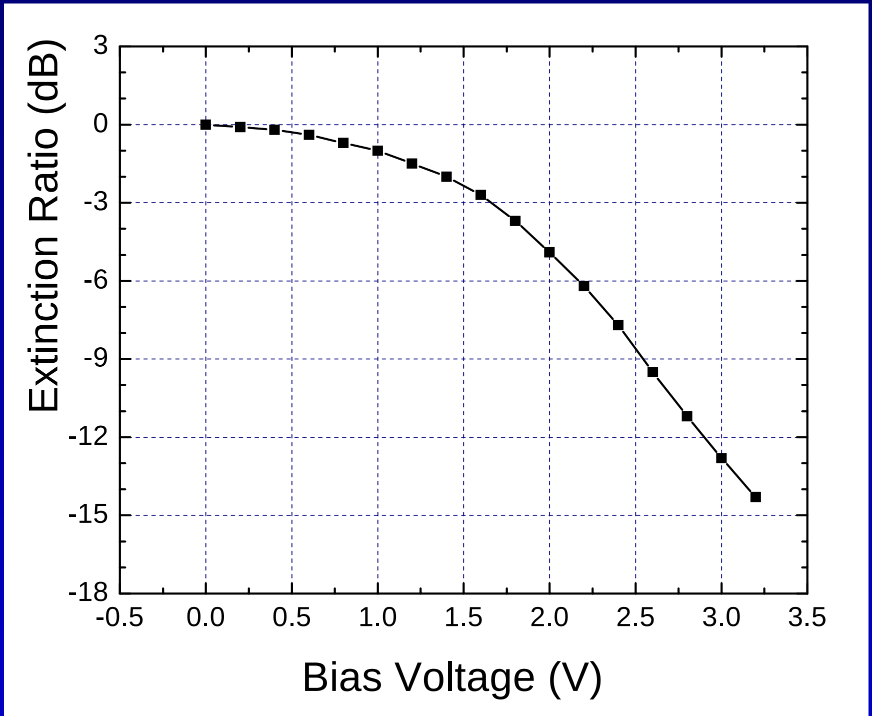
Xiong B, Wang J, Zhang L, et al. IEEE Photon. Technol. Lett. 2005, 17(2):327-329

Schematic of EA Modulator Integrated DFB Laser Diode



Static Performances of 40 GHz Integrated EMLs

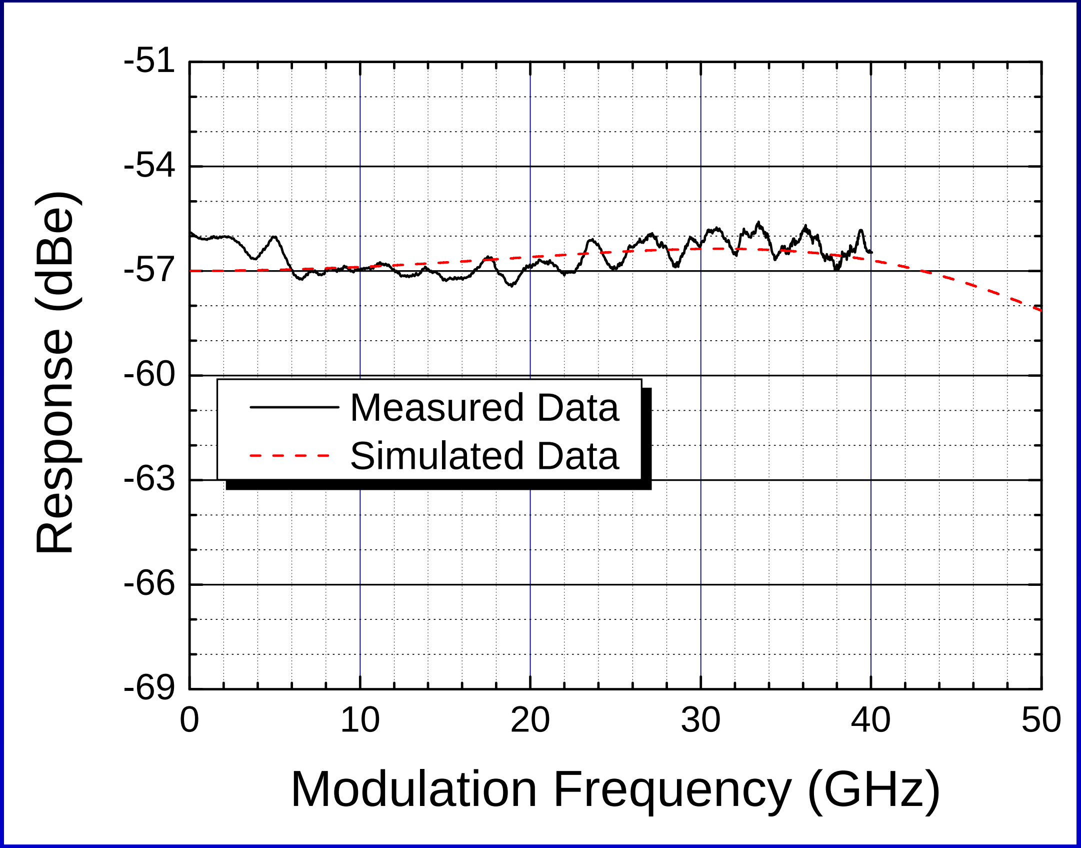




Light Power versus Current Curve
Very Low I_{th}= 12 mA

Static Extinction Ratio: 13 dB@-3V

Small Signal Modulation Response of 40 GHz Integrated EMLs



BW (3 dBe) > 40 GHz

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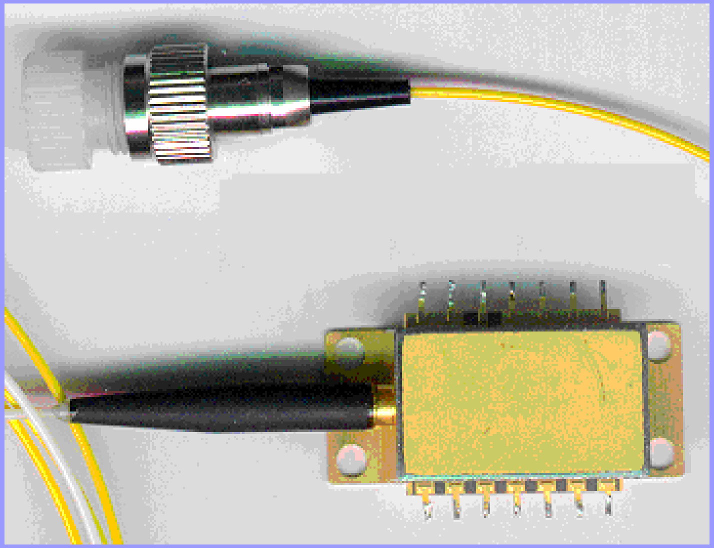
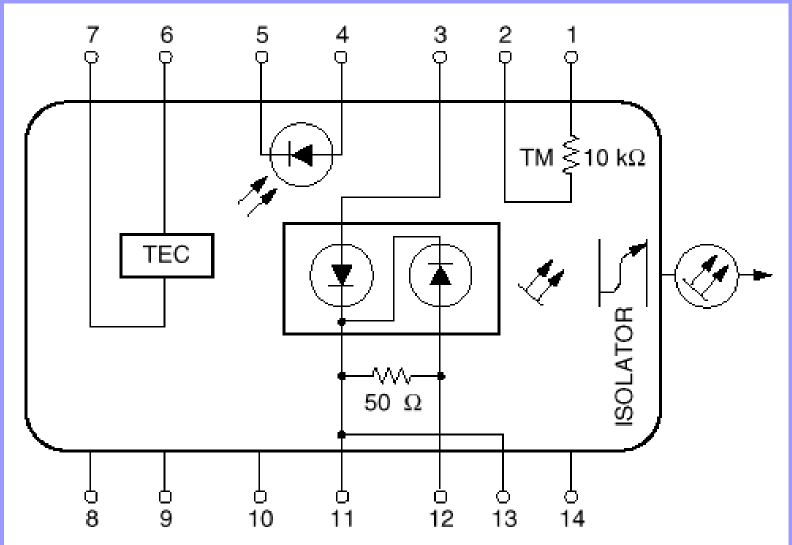
14-pin Butterfly Packaged Integrated Light Source Module

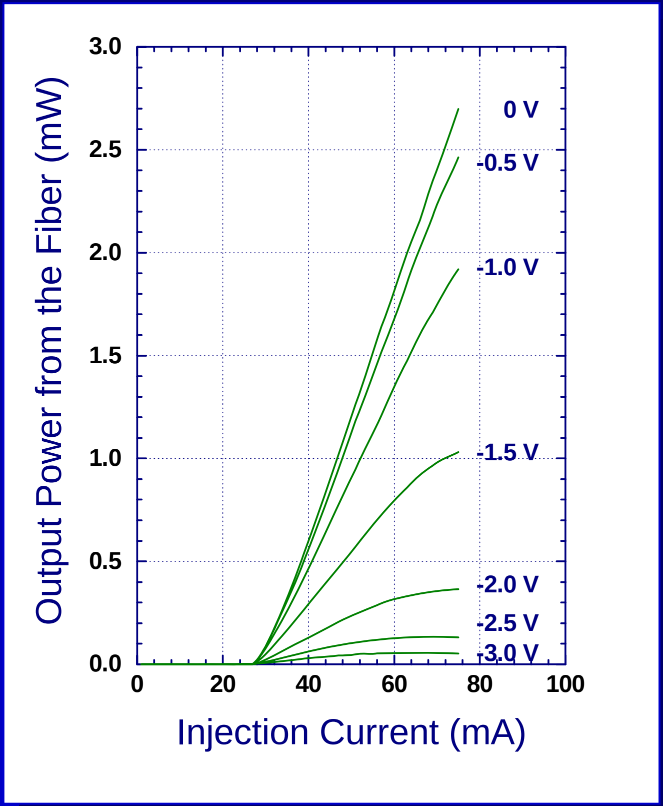


14-pin Butterfly Packaged Module

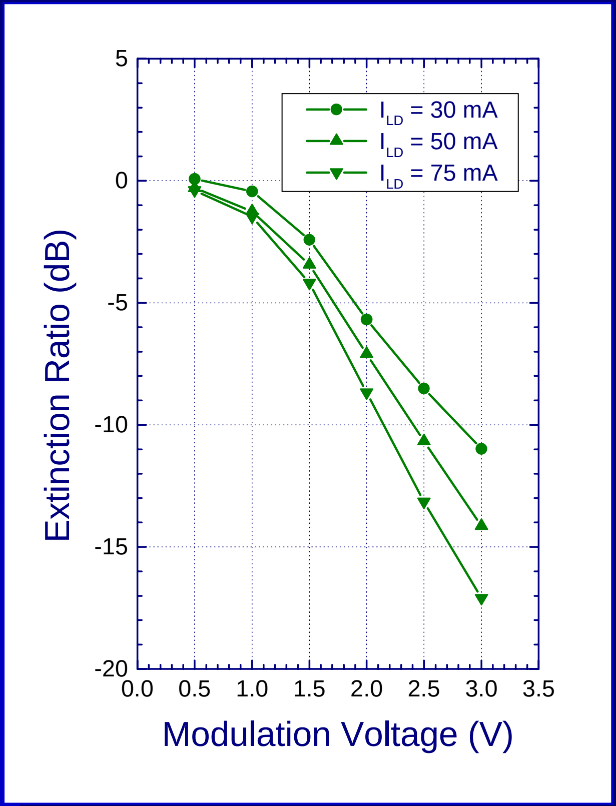


Circuit Schematic

Static Modulation Characteristics of Integrated Light Source Module

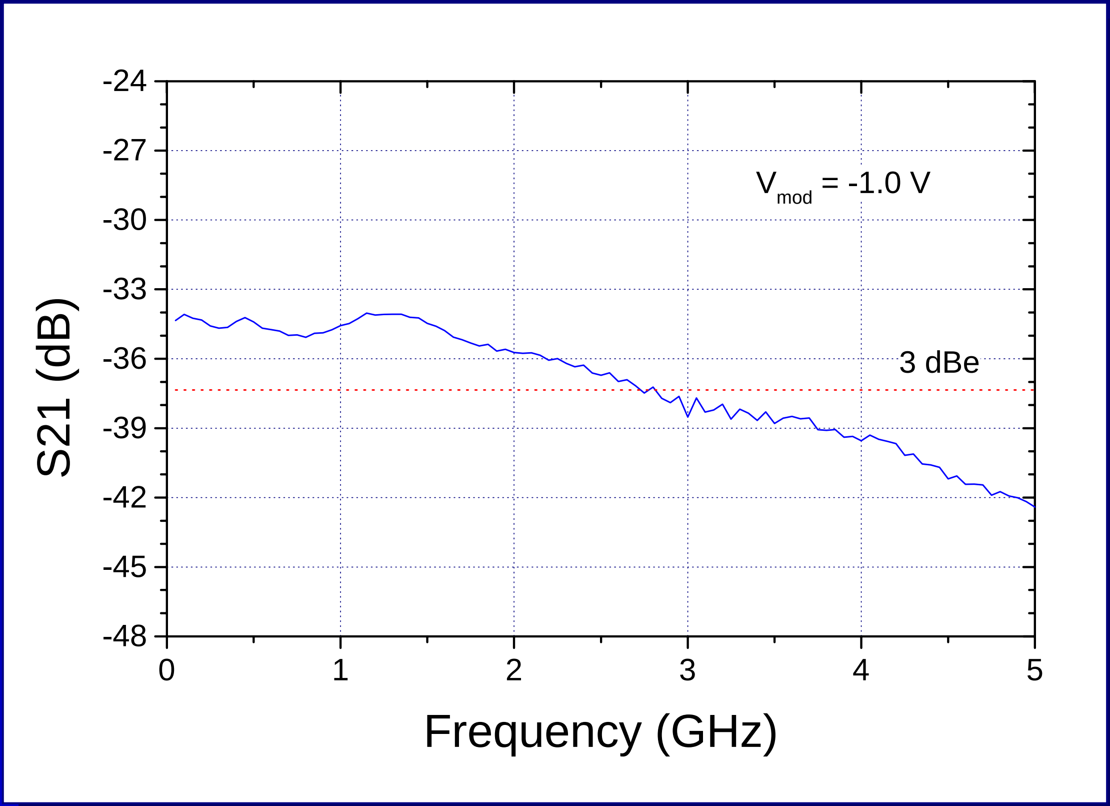


Threshold Current ~ 25 mA



Extinction Ratio > 15 dB

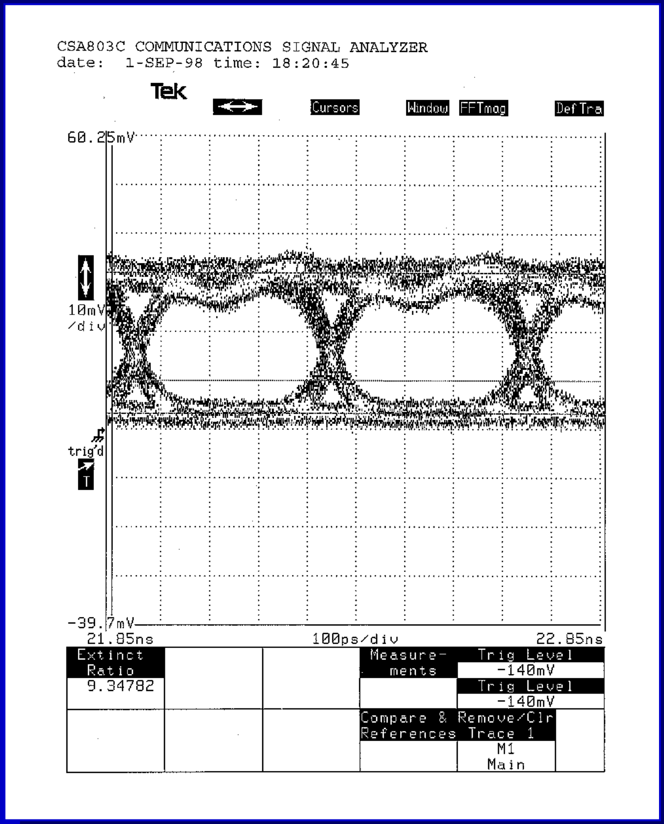
Small Signal Frequency Response



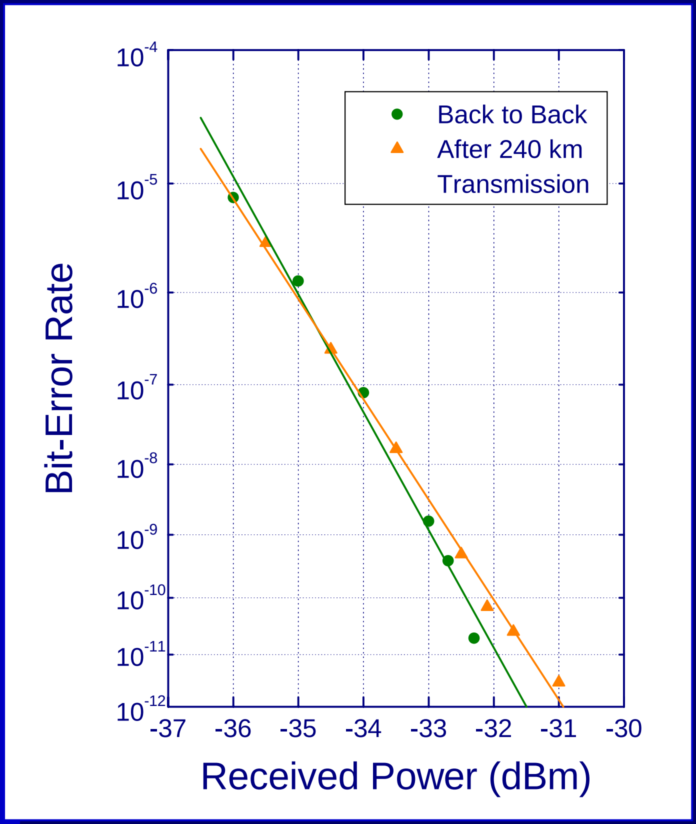
BW (3 dBe) ~ 3 GHz

Modulation bandwidth suitable for 2.5 Gb/s applications

Transmission Performance in 2.5 Gb/s WDM System

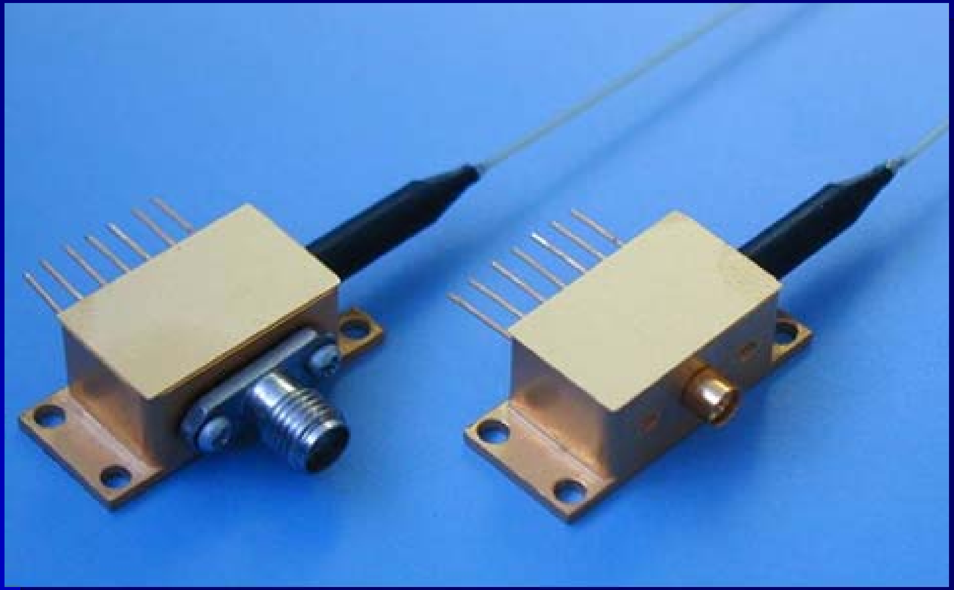


Back to Back Eye Diagram



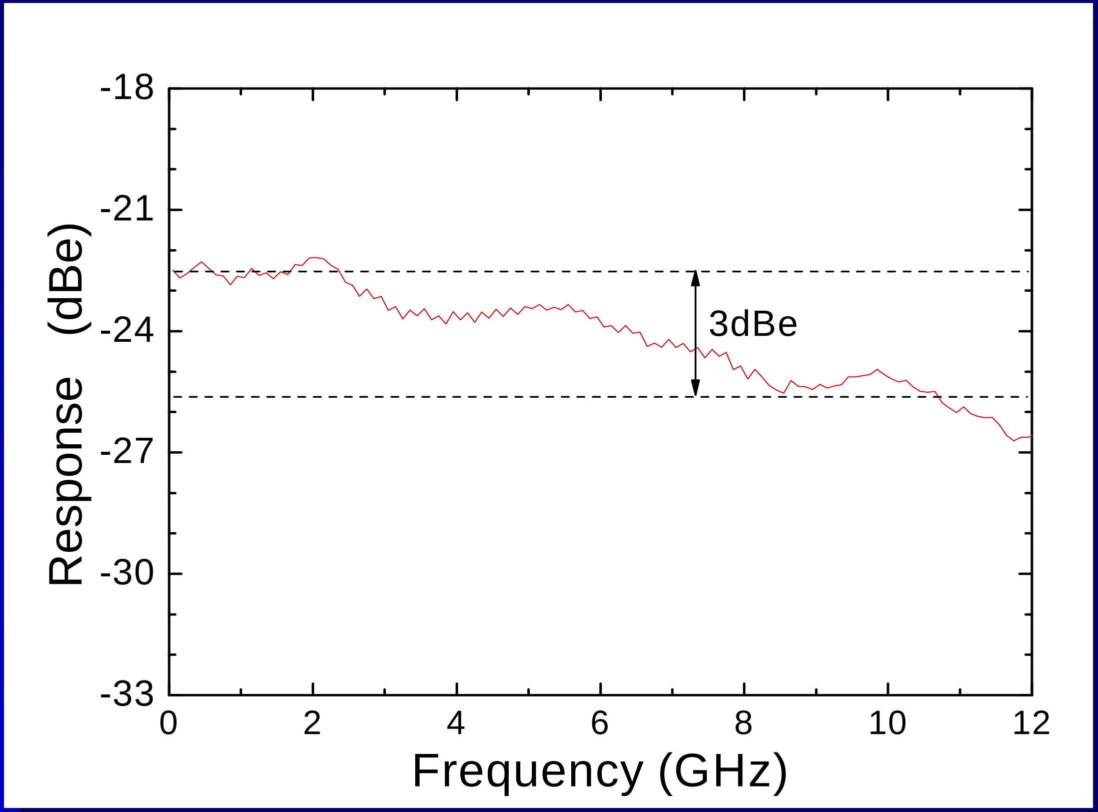
BER Performance

EML Module for 10 Gb/s Applications



K-connector or GPO connector
for Modulation Signal Input

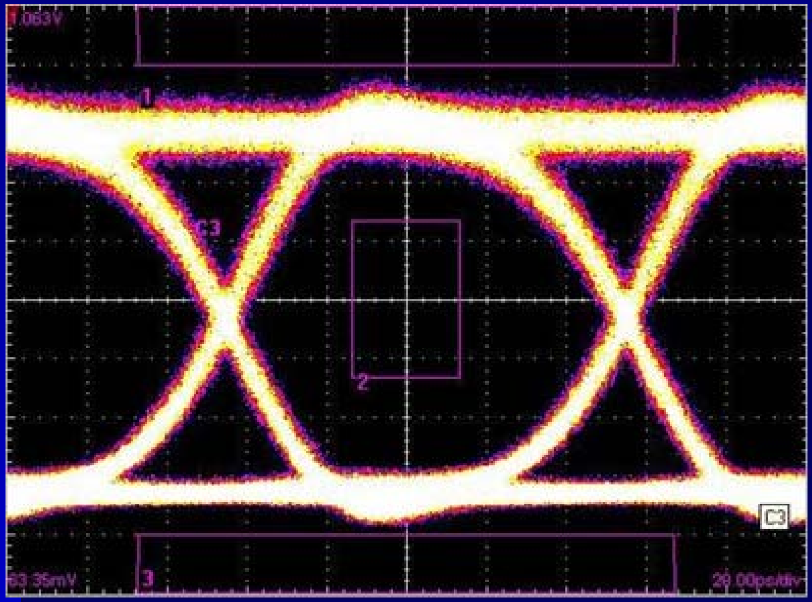
EML for 10 Gb/s Fiber Communications



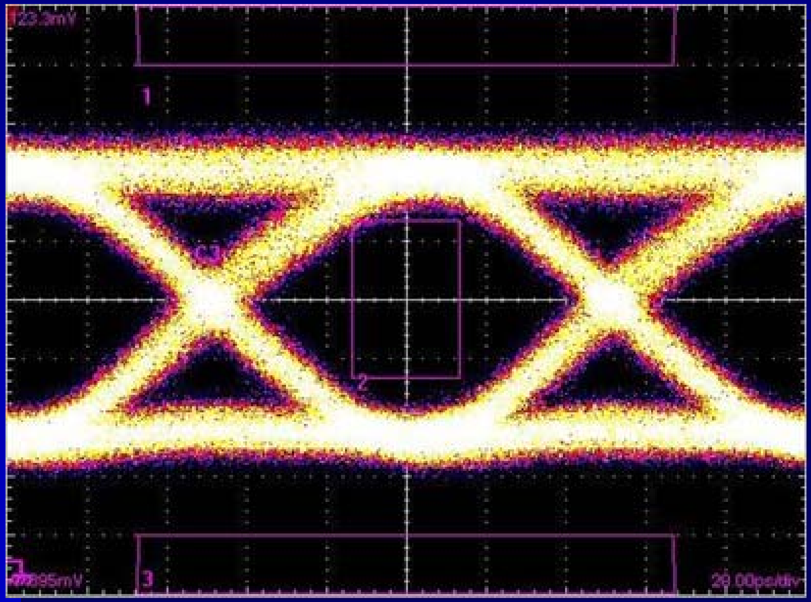
BW (3 dBe) > 10 GHz

Modulation bandwidth suitable for applications in 10 Gb/s systems

Eye Pattern Under 10 Gb/s NRZ PRBS Modulation

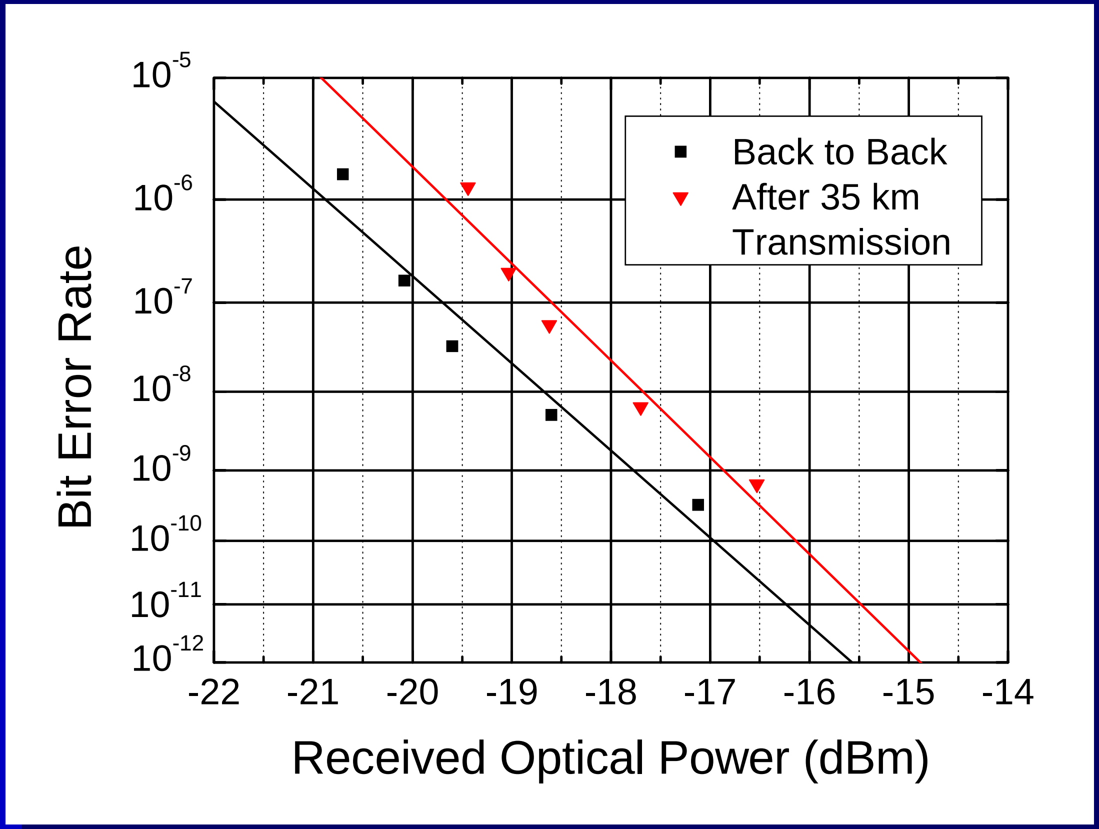


Back-to-Back



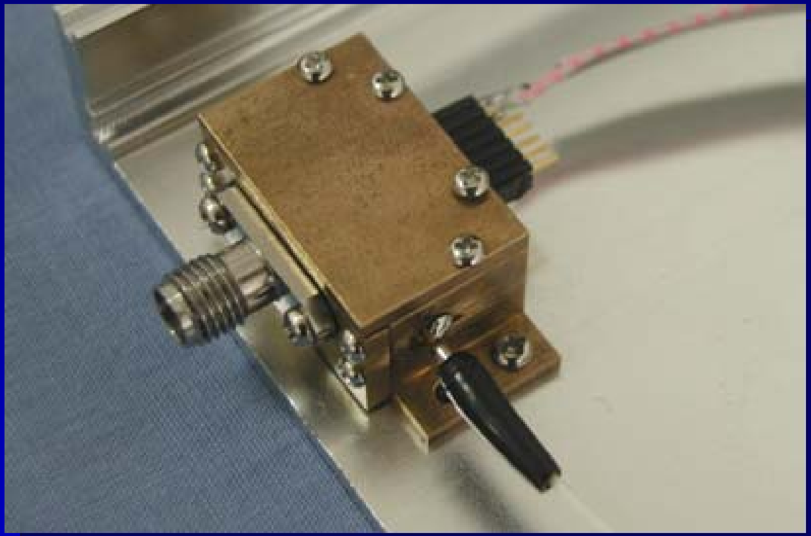
After Transmission Through 35 km SMF

Bit-Error-Rate Performance

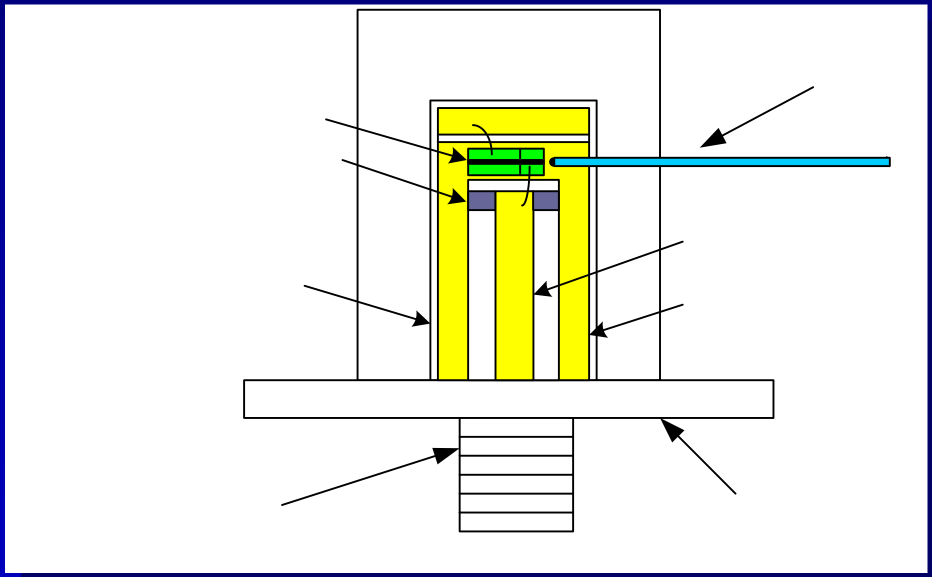


Power Penalty < 1 dB @ BER = 10^{-12}

40 Gb/s EML Transmitter Module

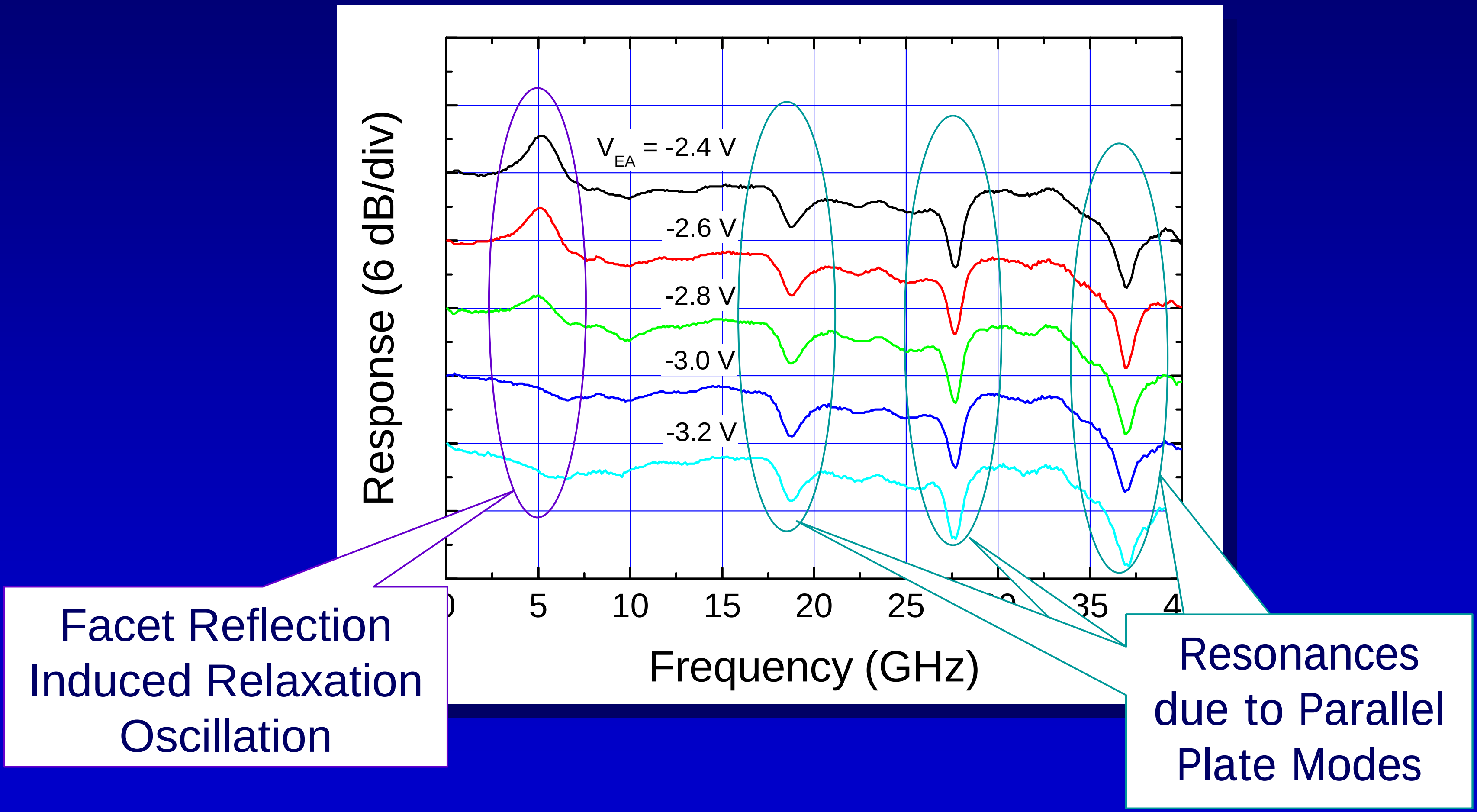


Prototype 40 Gb/s
Transmitter Module

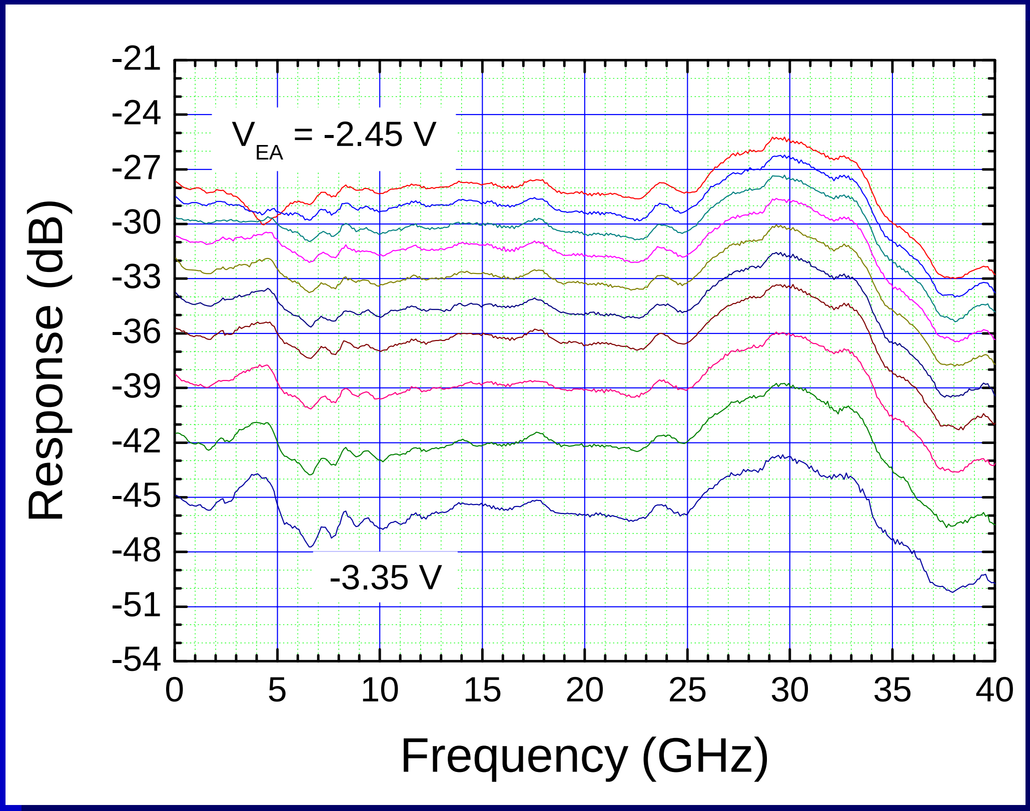


Inside View of 40 Gb/s
Transmitter Module

Resonances in Frequency Response of Packaged Module

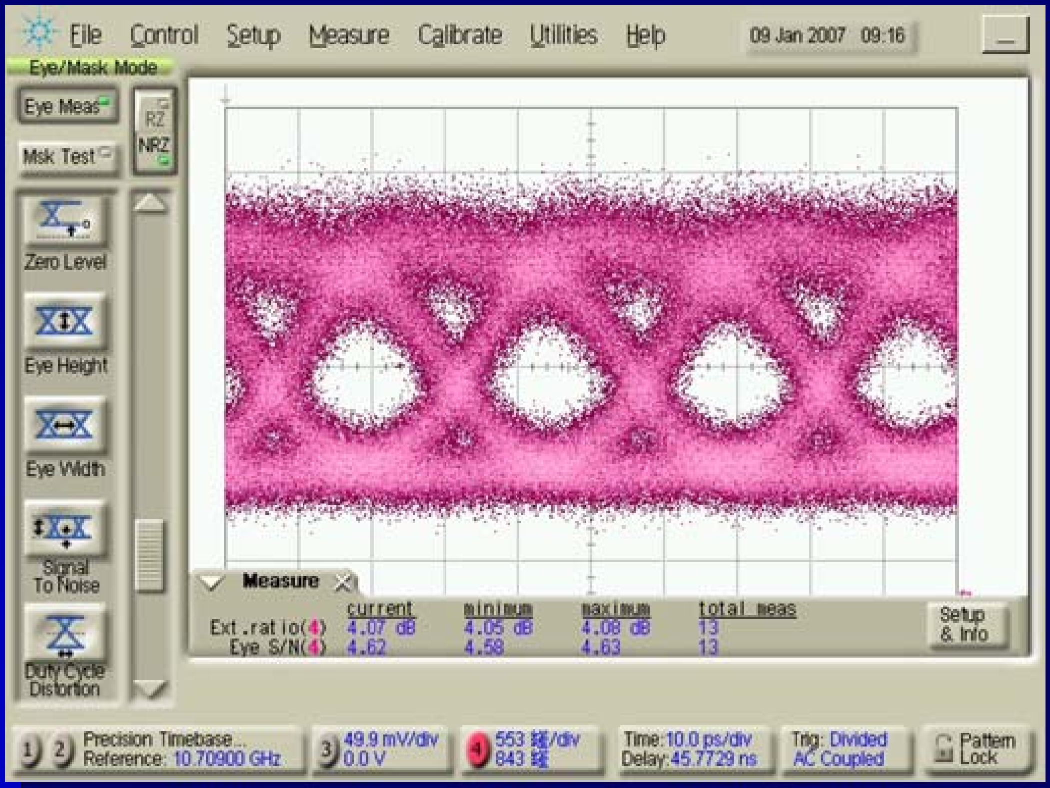


Suppression of Resonances in Frequency Response



After AR-coating & CPW Design Optimization

Large Signal Modulation Performance



Eye Diagram Under 40 Gb/s NRZ Pseudo-Random Bit Sequence Modulation ($V_{p\text{-}p}$ = 2 V)

Thanks for your attention