

超高速半导体器件与集成电路 发展与展望

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2007年10月11日

无线通信构建信息时代

卫星导航

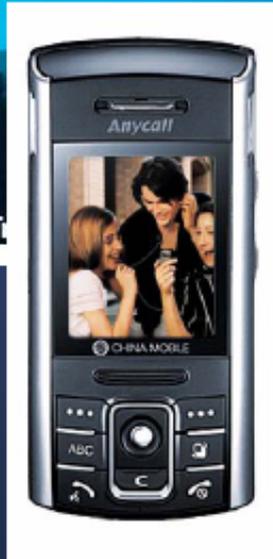


蓝牙耳机

通信基站



无线上网

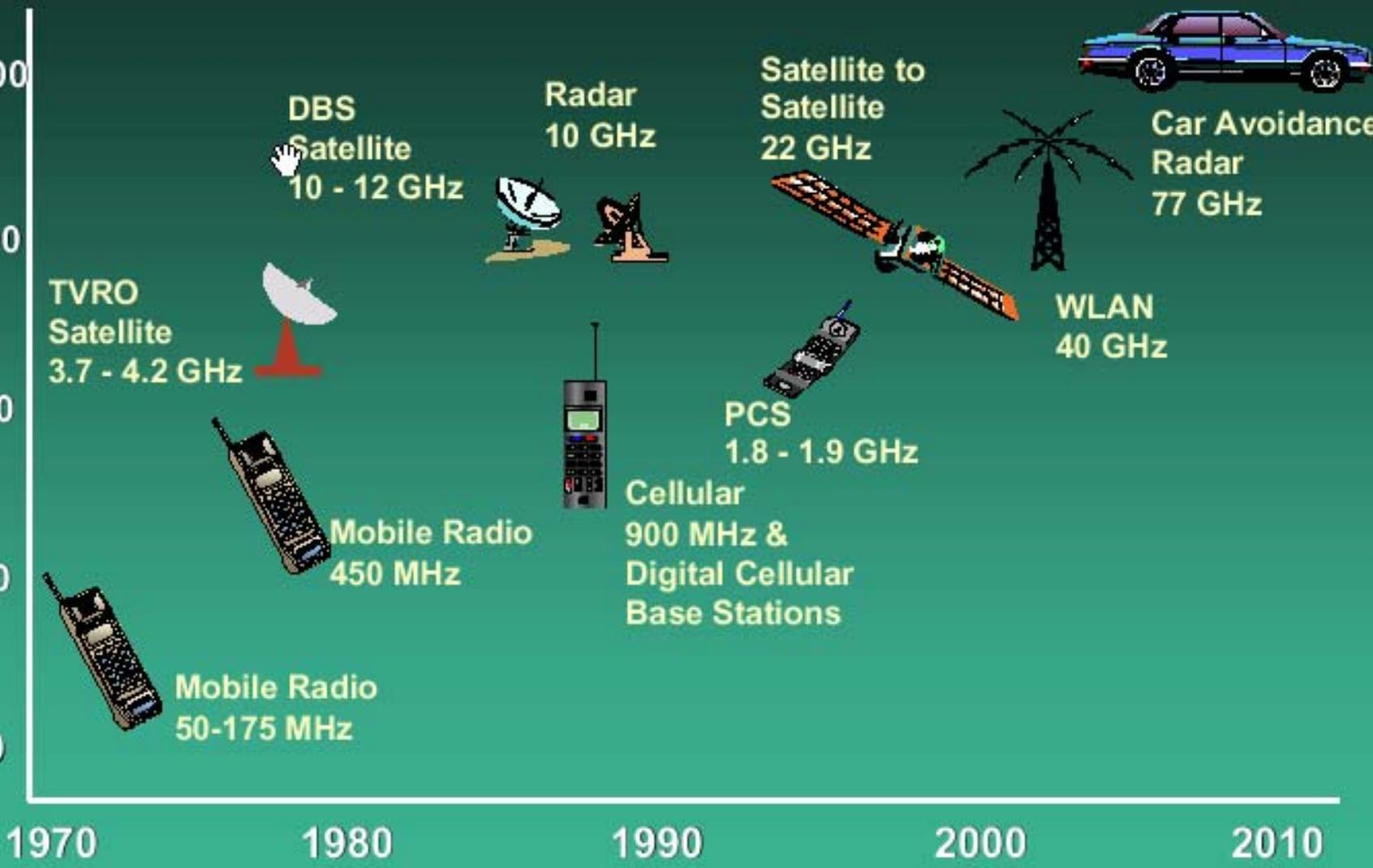


个人通信



MHz

100,000
10,000
1,000
100
10

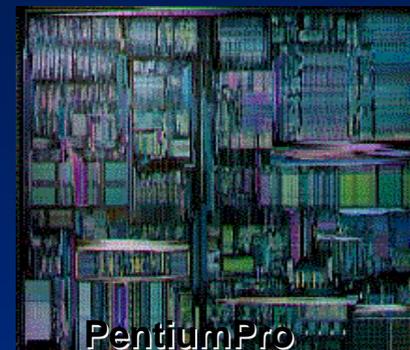


半导体器件与集成电路发展追求的目标

1947
Transistor



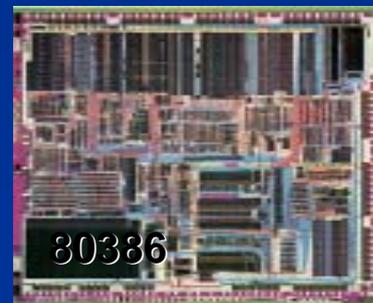
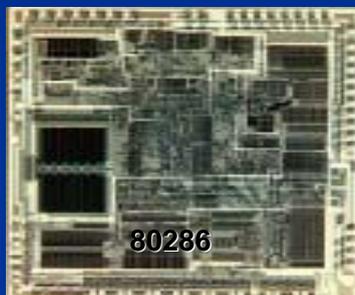
- 高速度
- 高密度
- 高可靠
- 低功耗



1200 k trans



29 k trans



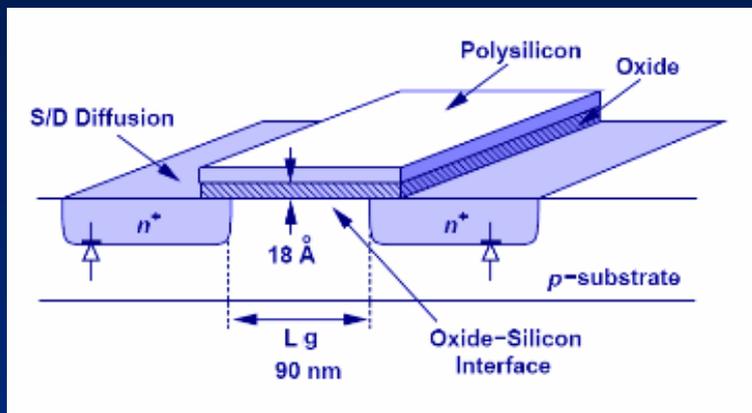
超高速器件和电路实现途径和方法

- 依靠特征尺寸的缩小
- 依靠设计技术的发展
- 依靠器件结构的变革
- 以靠新型材料的进步



**(一) 依靠特征尺寸的缩小
提高器件和电路的速度**

MOSFET的工作速度



□ 在半导体器件中,电子在电场作用下的运动速度 v_d :

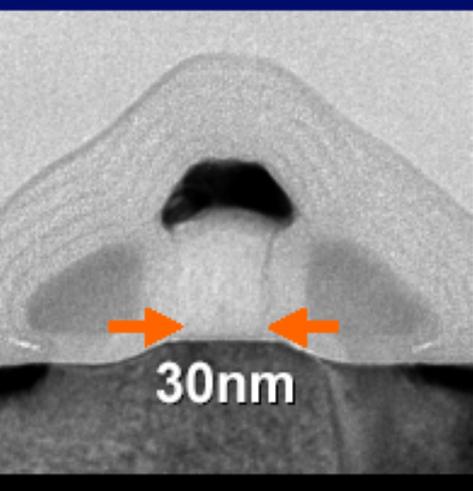
$$v_d = \mu_n E = \frac{\mu_n V_{ds}}{L_G}$$

□ MOS器件的特征频率 f_T :

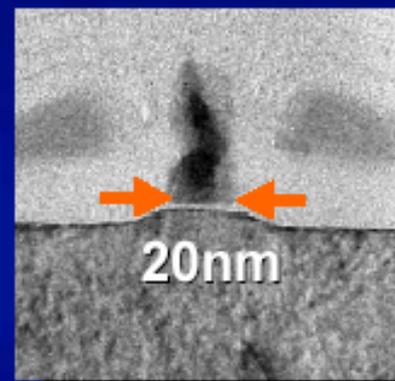
$$f_T \approx \frac{v_d}{2\pi L_G} = \frac{\mu_n V_{ds}}{2\pi L_G^2}$$

Intel's Transistor Research In Deep Nanotechnology Space

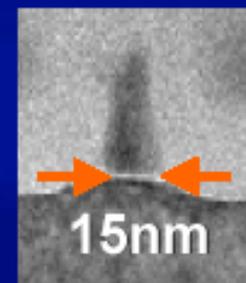
Experimental transistors for future process generations



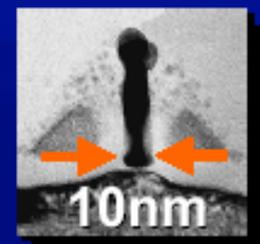
65nm process
2005 production



45nm process
2007 production



32nm process
2009 production

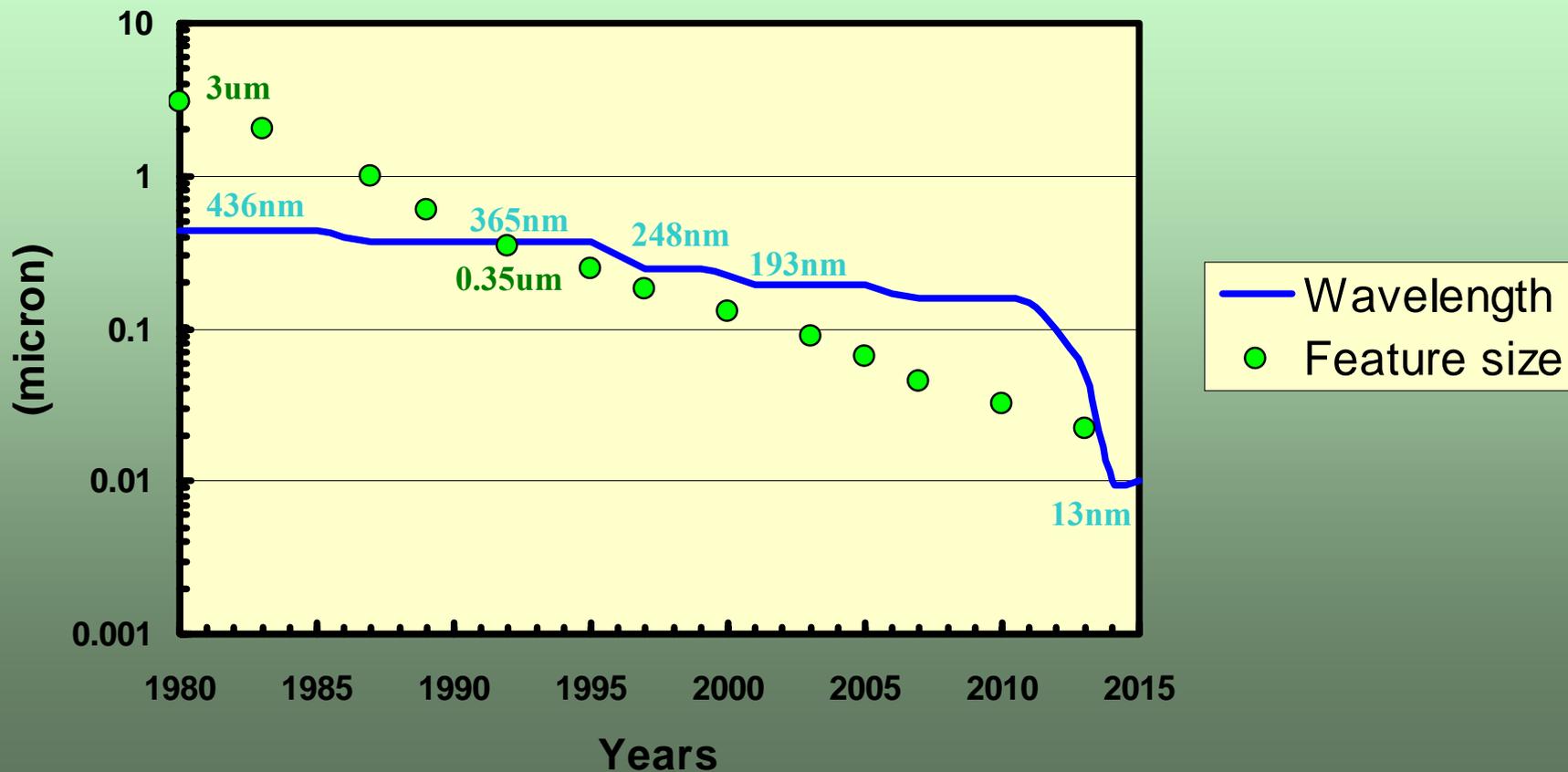


22nm process
2011 production

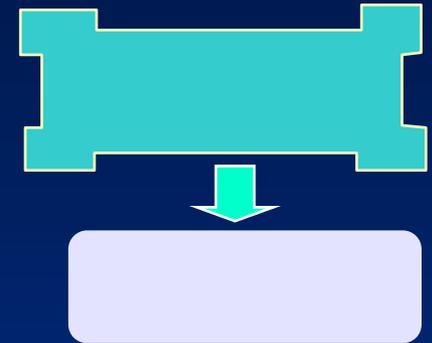
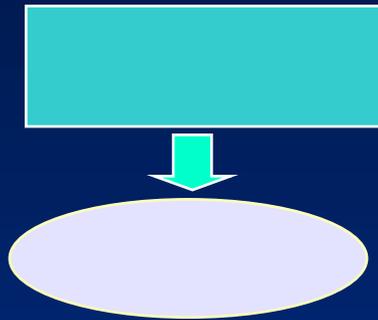
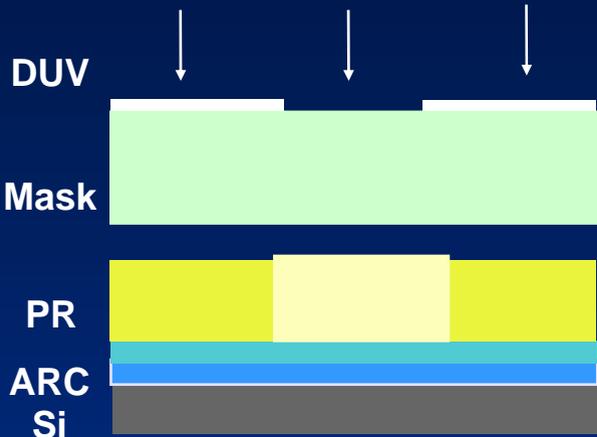
Transistors will be improved
for production

The Lithography light source wave length and Print image feature dimension

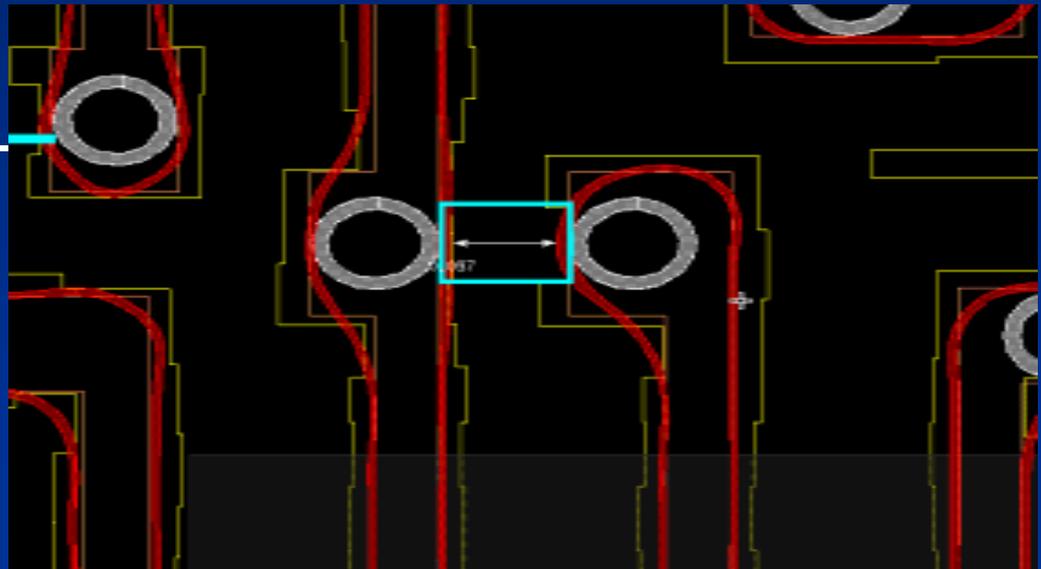
The lithography light source wave length and print image feature dimension



Lithography: phase shift, OPC



Optical proximity correction (OPC),
Rule based and model based



互连问题严重

在射频下，片上互电磁效应显著。

No single tool is able to solve all.

2 & 3-D Field Solvers

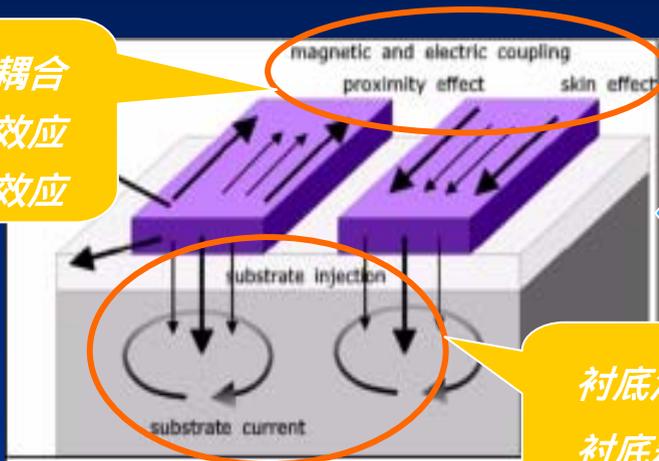
Transmission Lines

Solution Complexity
Speed-down
Accuracy

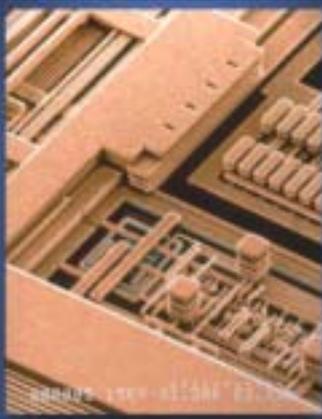
RLC

DC 10.0 40.0 100 200 GHz

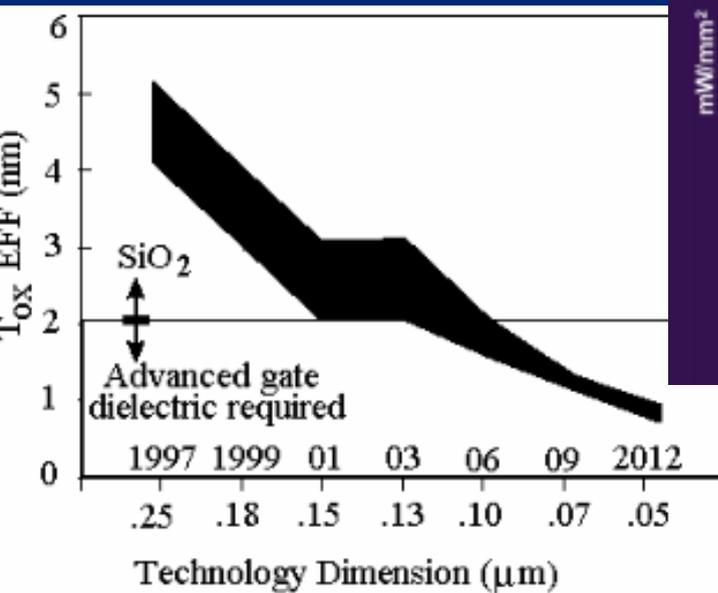
电磁耦合
邻近效应
趋肤效应



衬底注入
衬底耦合

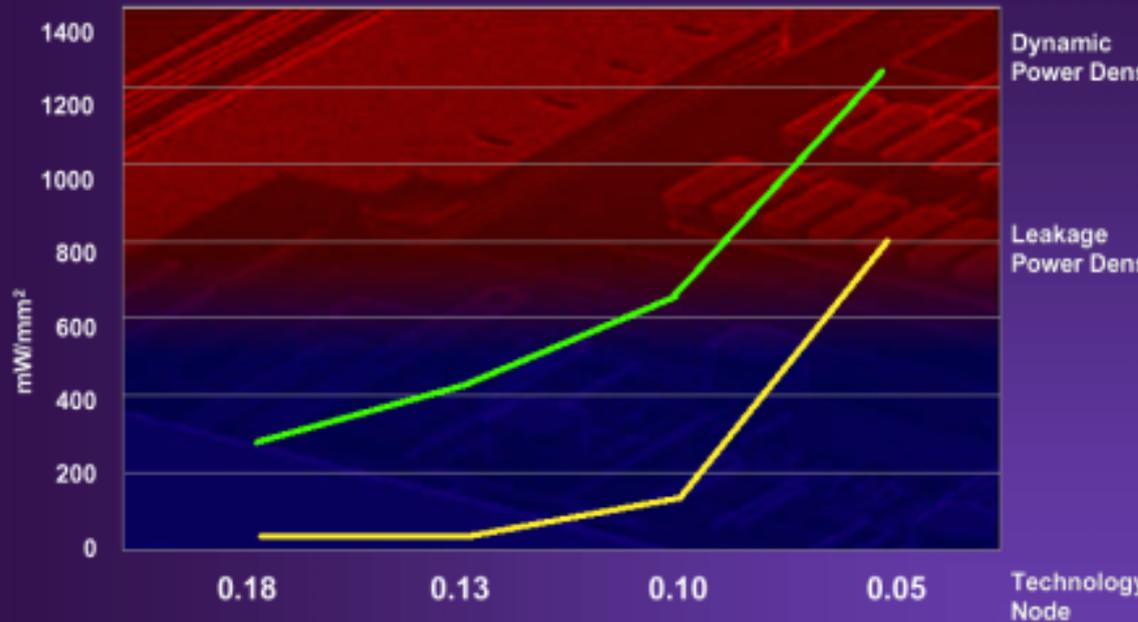


栅氧厚度和静态漏电问题



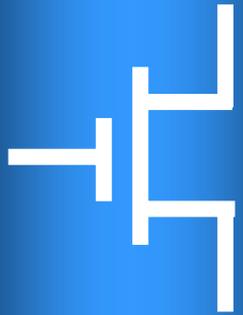
ITRS roadmap for gate dielectric thickness.

Design for Low Power: Power Leakage



The Great Techonomics Shake-up

Technology



Economics



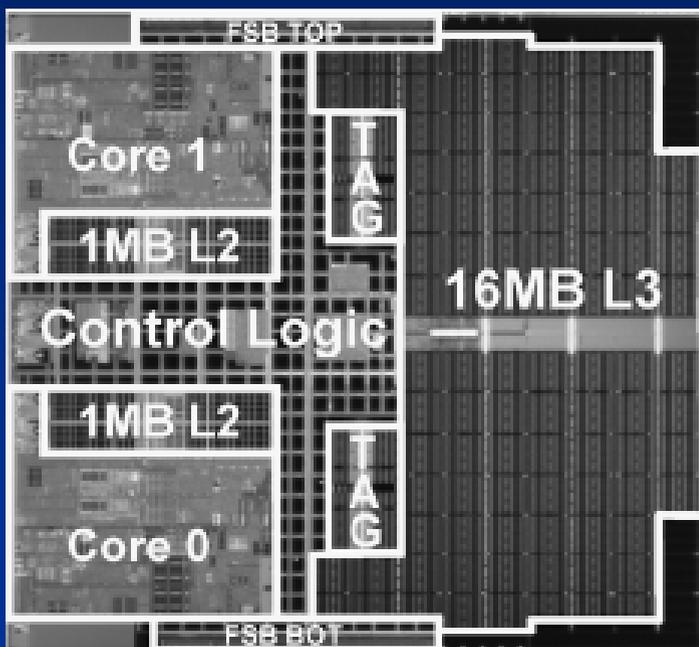
Techonomics!



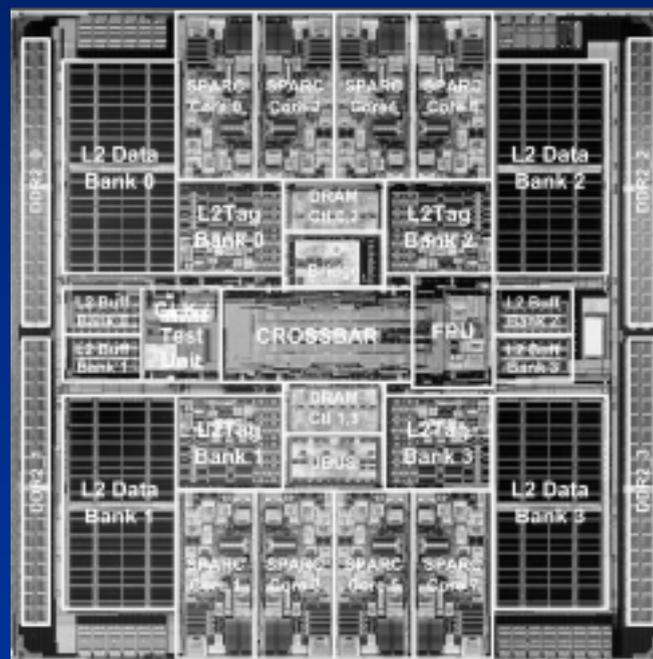
**(二) 依靠设计技术的发展
提高集成电路的速度**

超高速IC技术发展趋势（1）

1、共享存储器的多核结构

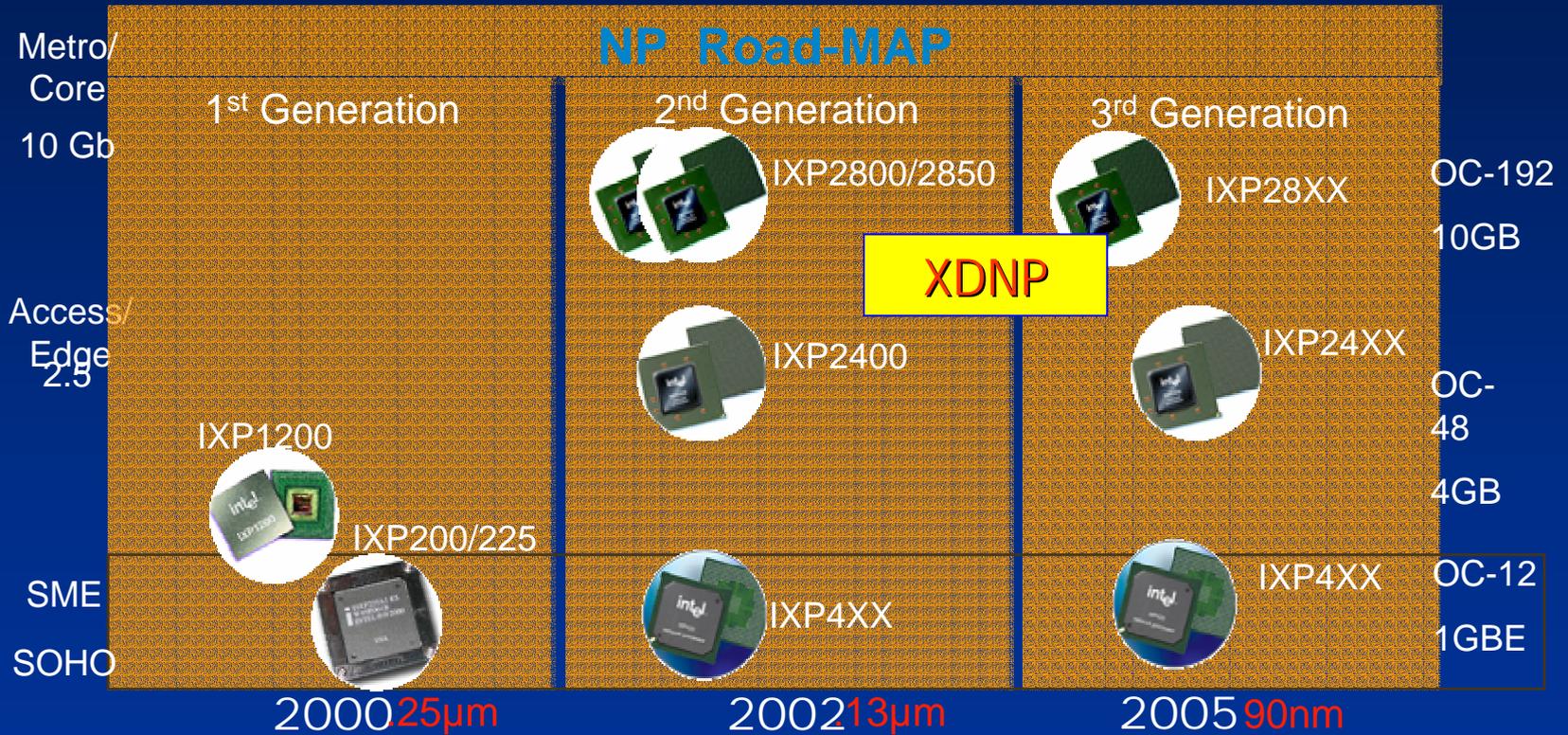


Intel公司Xeron 2核共享存储器



Sun公司SPARC 8核CPU版图

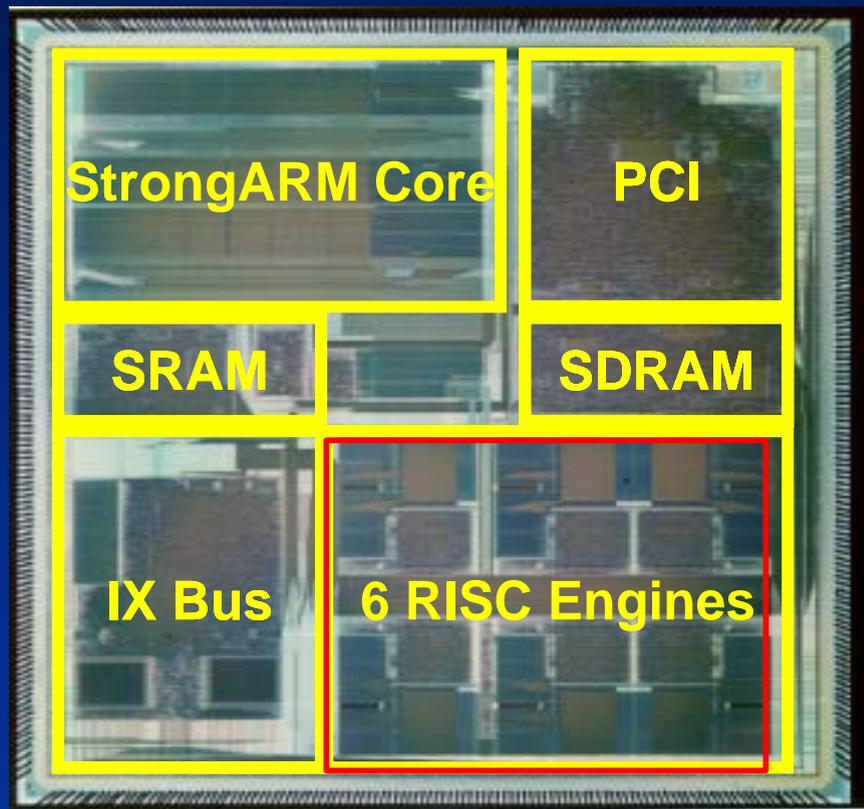
网络处理器芯片发展



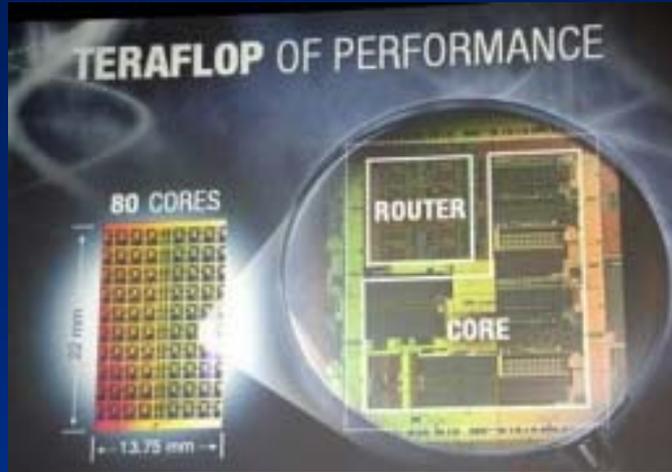
NP技术发展

XDNP多核处理器结构

- (1) 处理器是一种典型的同构多核处理器结构；
- (2) 增加交换内核数量是提高NP交换能力的一种重要途径，



2、分享存储器的多核结构



Intel公司Tera-Scale 80核处理器

- ❖ 65nm SOI 工艺，275平方毫米
- ❖ 主频3.16GHz，电压0.95V
- ❖ 功耗62W
- ❖ 32位非X86结构
- ❖ 浮点运算能力1.01TFloFs（每秒万亿次）
- ❖ 相当于1万颗Pentium Pro 运算能力



超高速IC技术发展趋势（2）

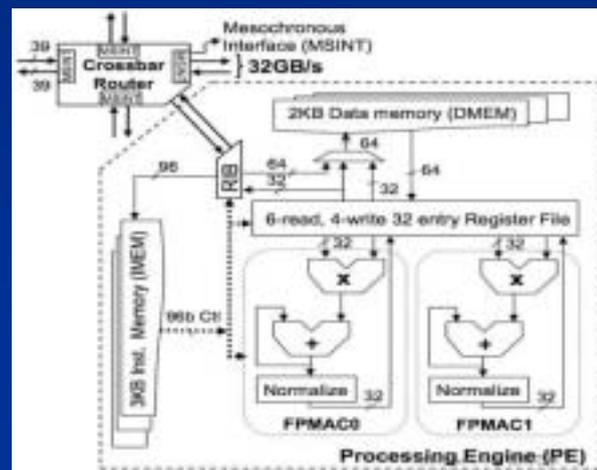
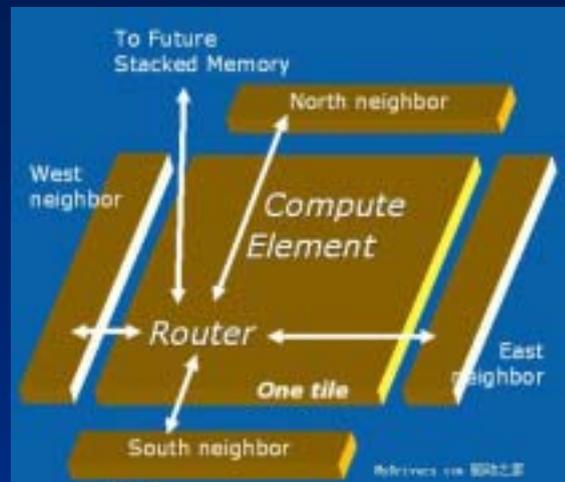
多核处理器单核结构的发展

特点：

- (1)增加了用于数据交换的网络通信接口；
- (2)采用共享存储器技术减小单核专用存储器面积；
- (3)网络通信用于内核之间的互连。

优势：

- (1)通用内核的使用缩短芯片开发周期
- (2)灵活的设计，研发人员少
- (3)分布式运算，极大提高系统运算能力



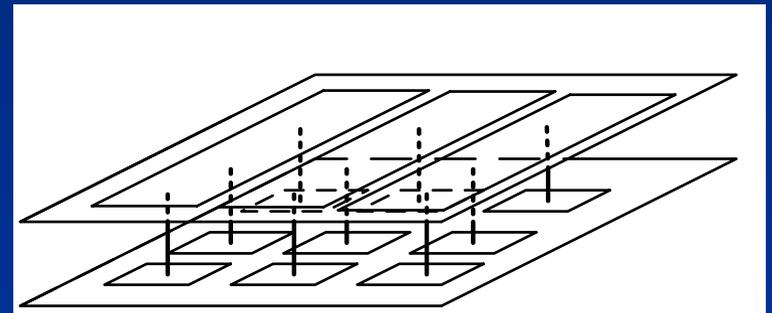
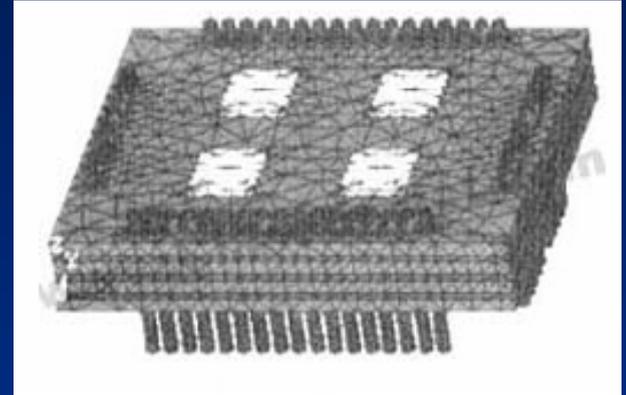
典型多核芯片的单核电路结构

超高速IC技术发展趋势 (3)

新型存储器结构

存储器已经成为SoC芯片的主要单元，在NP和通用CPU中，存储器占用面积已经超过50%。随着芯片和内核数量的增加，存储器占用比例还会继续增加。

新一代存储器正向三维存储器结构和共享存储器结构发展。

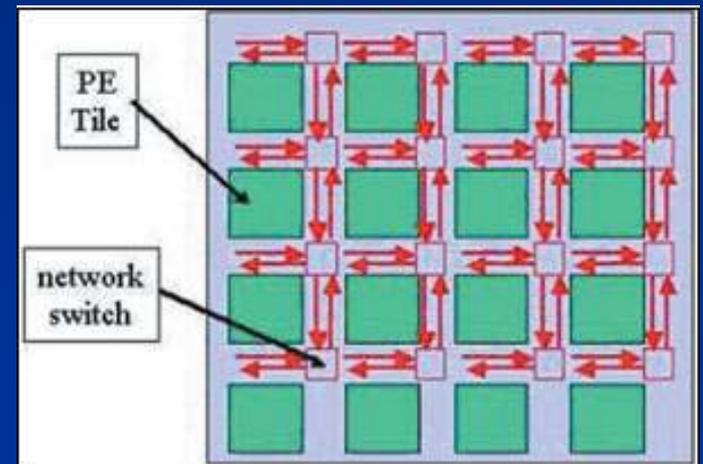
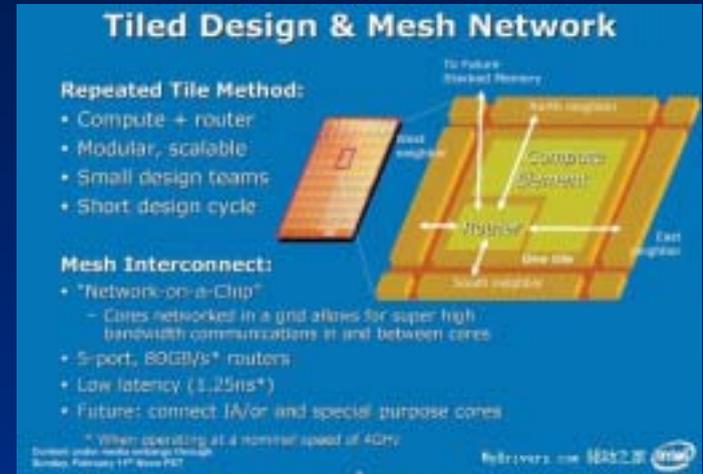


三维存储器结构

高速IC技术发展趋势（4）

新型总线互连技术NoC

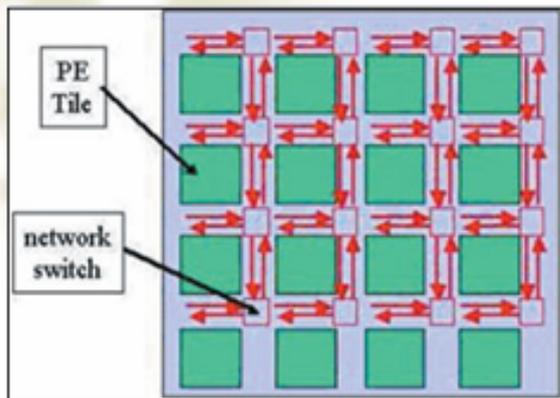
SoC芯片面积的增加，使得芯片全局一致性降低，无法满足超大规模集成电路芯片高频率工作要求。在新一代的处理器中，开始采用基于路由和交换技术的网络互连技术(NoC)，作为芯片内核互连解决方案。



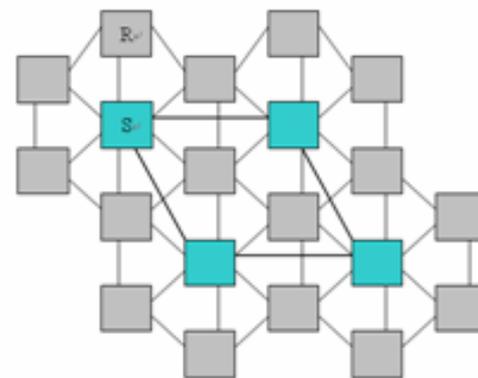
NOC拓扑结构



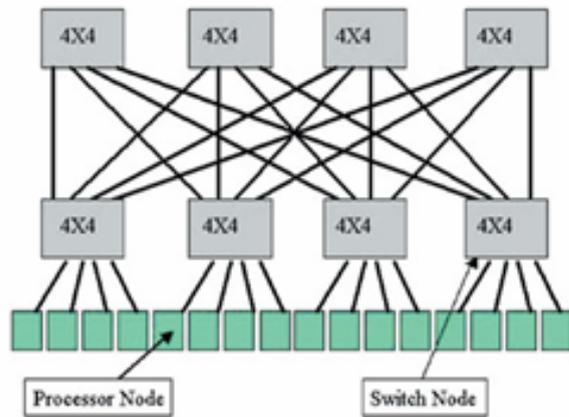
NOC拓扑结构



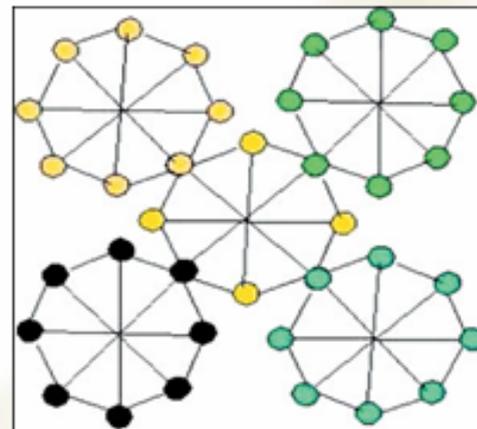
2维网状结构



蜂窝状结构



胖树结构

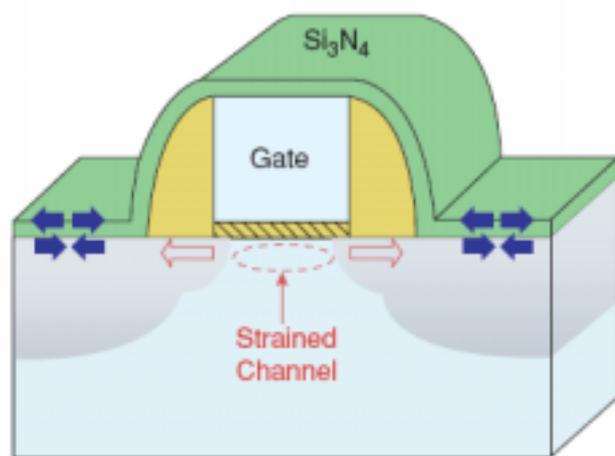


八角形网络

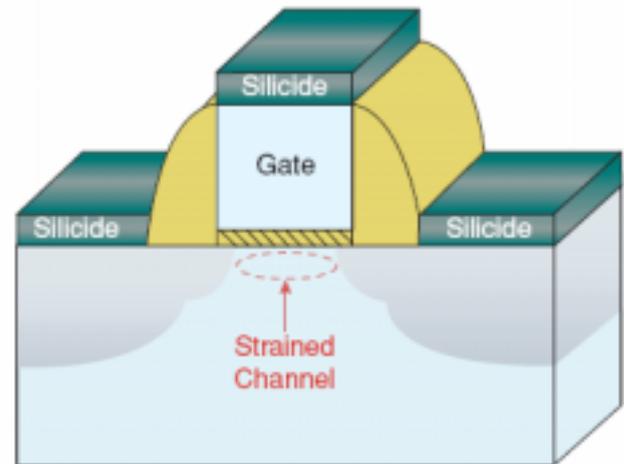
蚁群算法

**(三) 依靠器件结构的变革
提高器件和电路的速度**

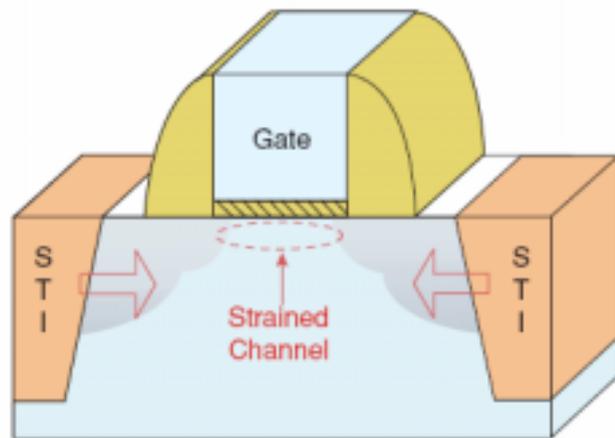
(一) 应变硅技术



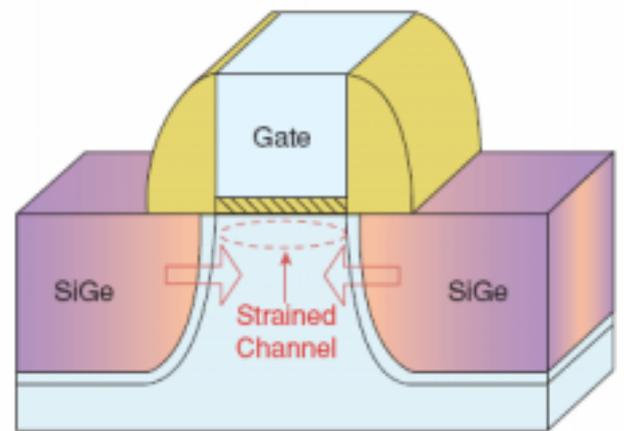
(a)



(b)

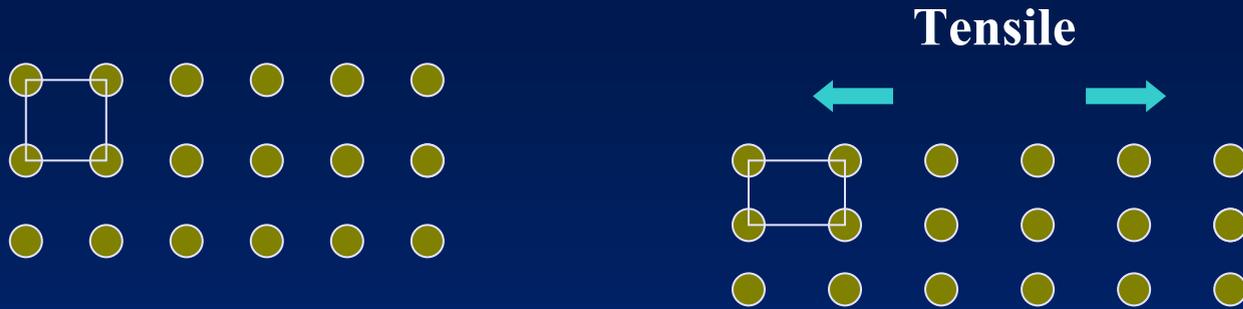


(c)

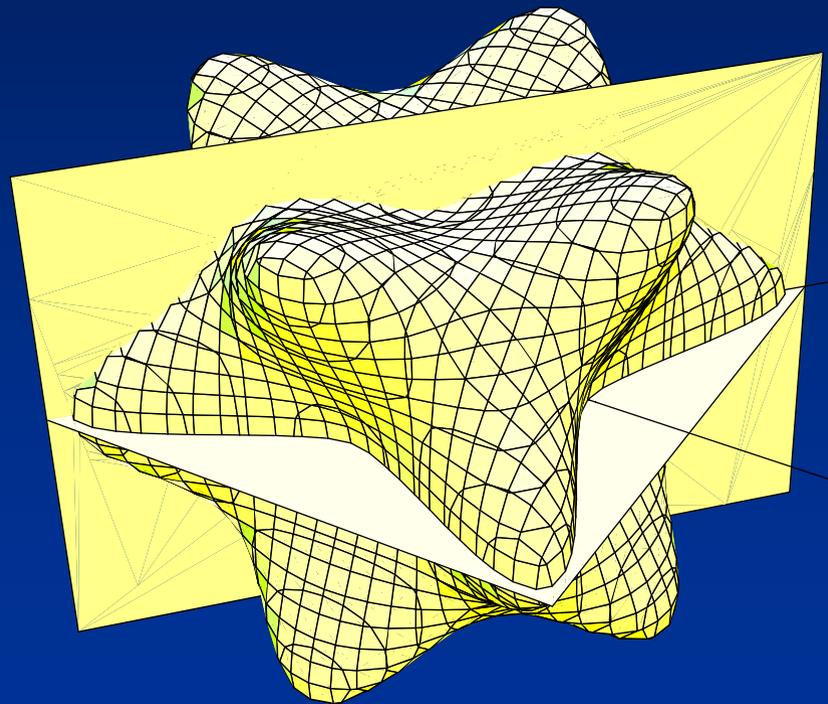
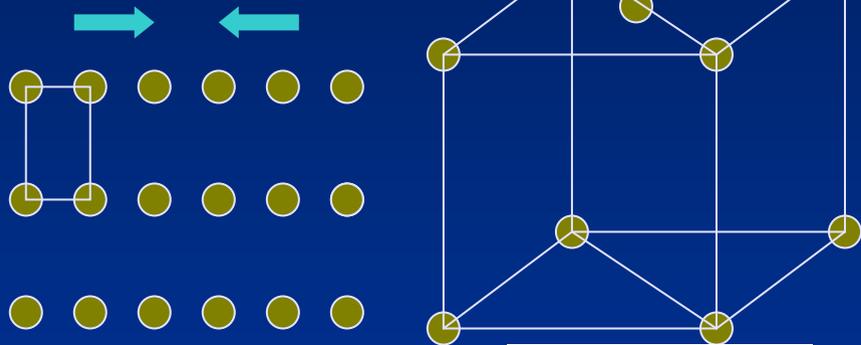


(d)

应变硅技术



Compressive



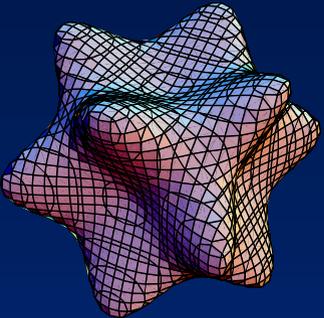
$$E_k = \frac{\hbar^2 k^2}{2m^*}$$

The symmetric of crystal

- ▶ The band structure
- ▶ The effective carrier mass
- ▶ The carrier mobility

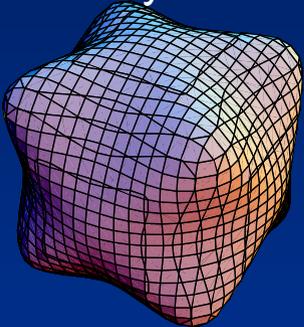
The transistor is facing to more and more stress just like a electrical engineer

Band Structure of Holes



heavy hole

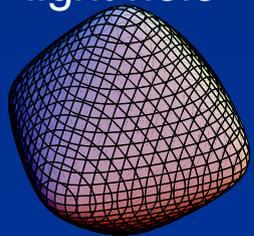
$$b_1 = 2\pi \frac{a_2 \times a_3}{a_1 \cdot a_2 \times a_3}$$



light hole

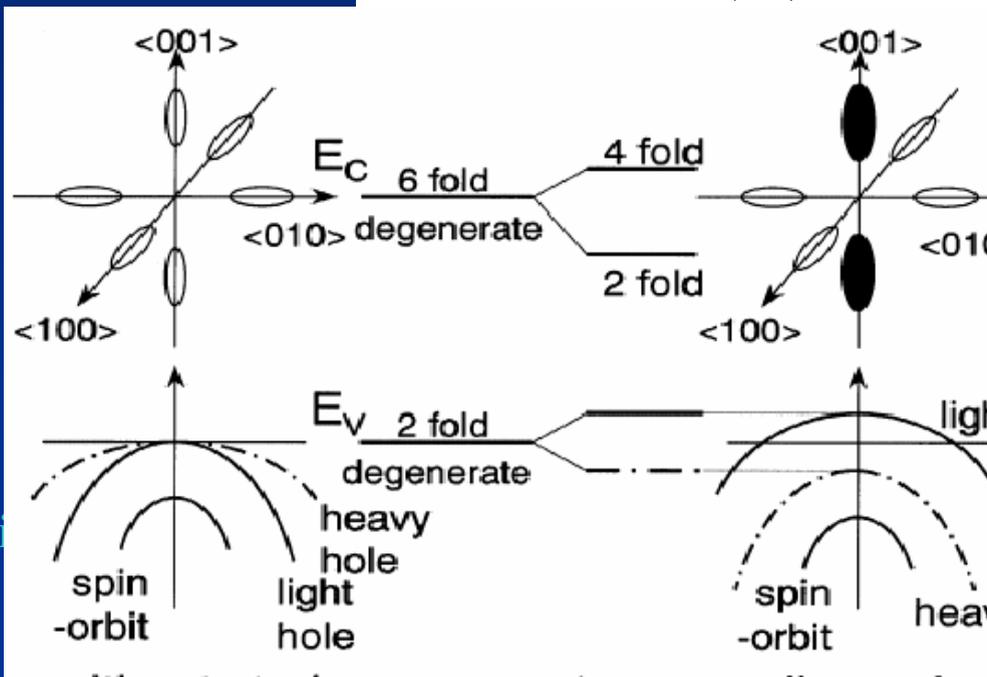
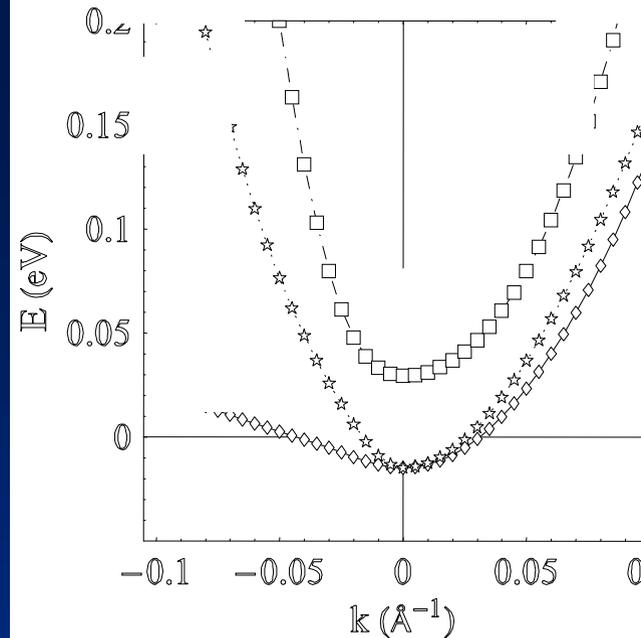
$$b_2 = 2\pi \frac{a_3 \times a_1}{a_1 \cdot a_2 \times a_3}$$

$$b_3 = 2\pi \frac{a_1 \times a_2}{a_1 \cdot a_2 \times a_3}$$

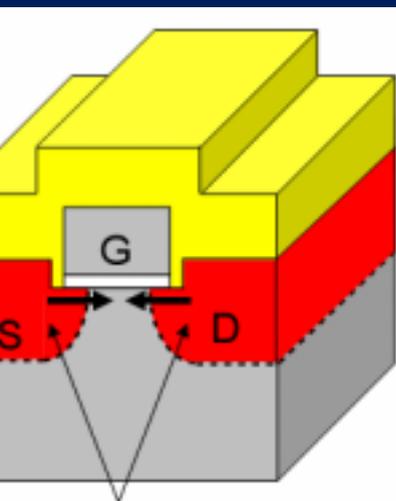


spin orbit hole

Reciprocal lattice

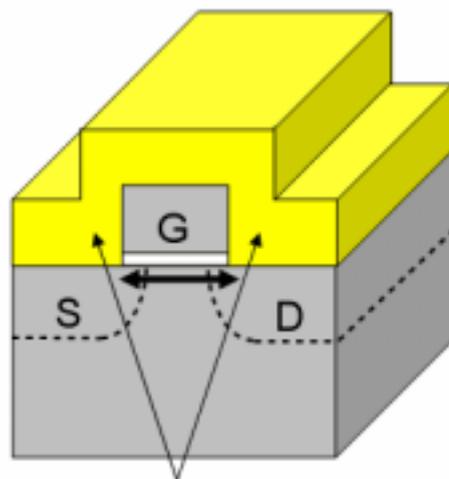


不同的应变引入方法



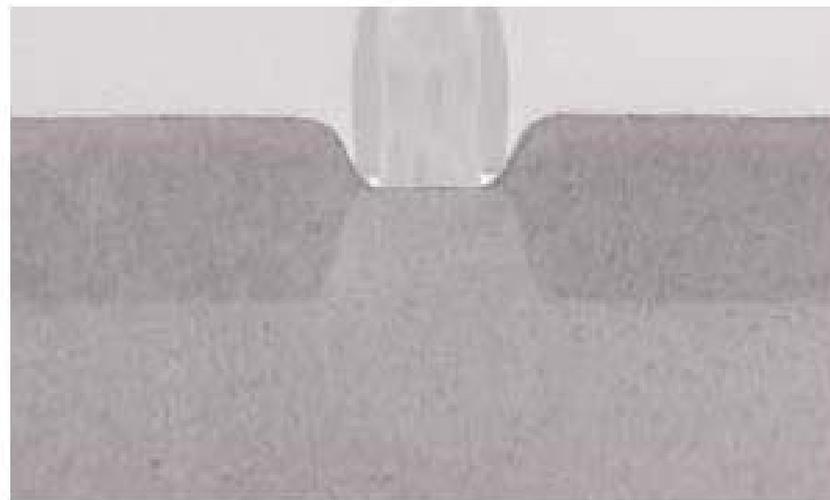
Selective SiGe S-D

Uniaxial
Compressive Strain
for PMOS



Tensile Si₃N₄ Cap

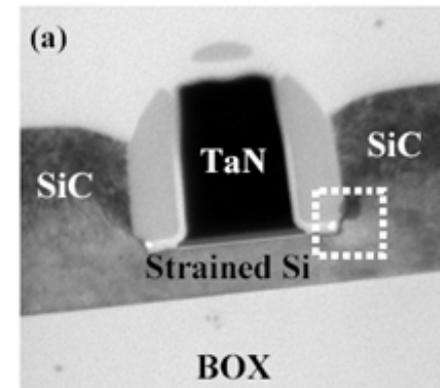
Uniaxial
Tensile Strain
for NMOS



在nMOS晶体管的S/D区域内选择生长高质量、无缺陷的SiC（含1.6%的碳）外延薄膜。使用循环淀积和刻蚀（cyclic-deposition and etch, CDE）工艺可以获得高的碳含量和高选择性。（来源：ASM）

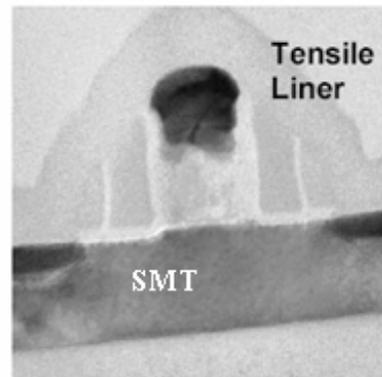
NMOS Stressors

Uniaxial



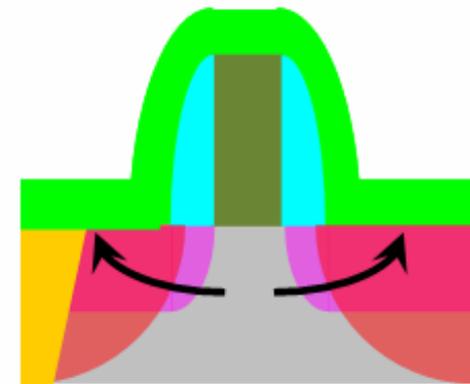
eSiC

Ang, et al, IEDM 2005



Stress Memory Technique

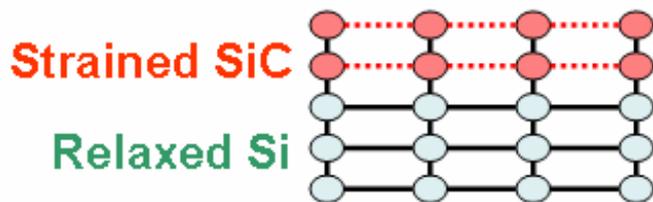
Horstmann, et al, IEDM 2005



t-ESL

Grudowski, et al, VLSI 2000

Biaxial



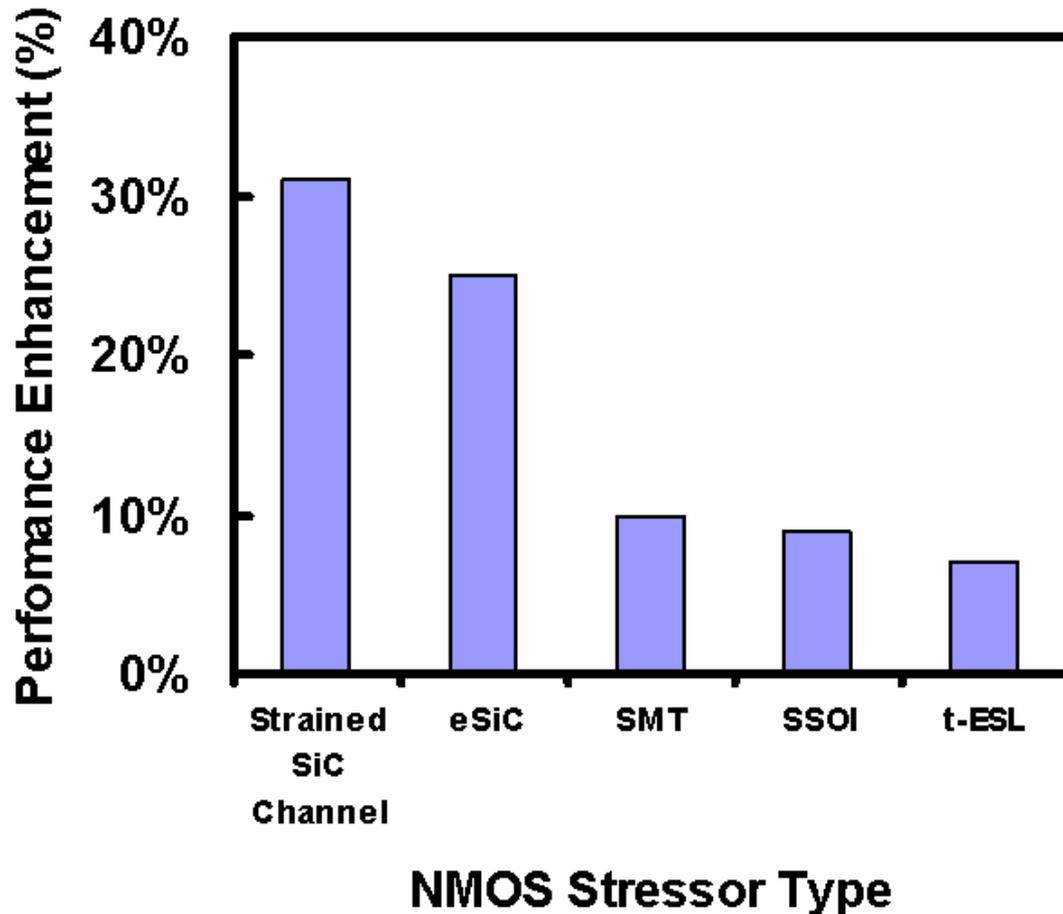
Strained SiC Channel
Ernst, et al, VLSI 2003



SSOI
Thean, et al, VLSI 2005

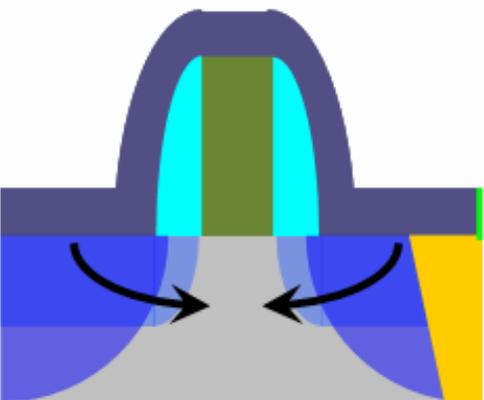
Strain Engineering

NMOS stressors



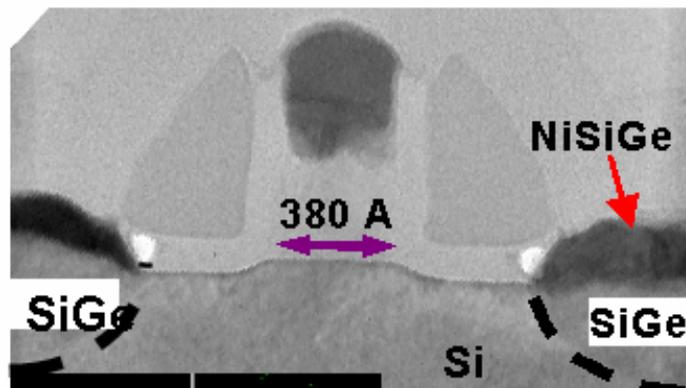
PMOS stressors

Uniaxial



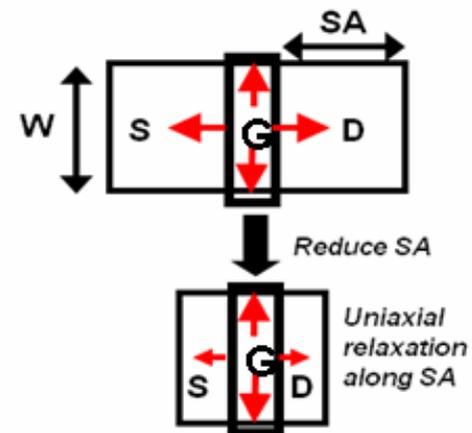
c-ESL

rudowski, et al, VLSI 2006



eSiGe

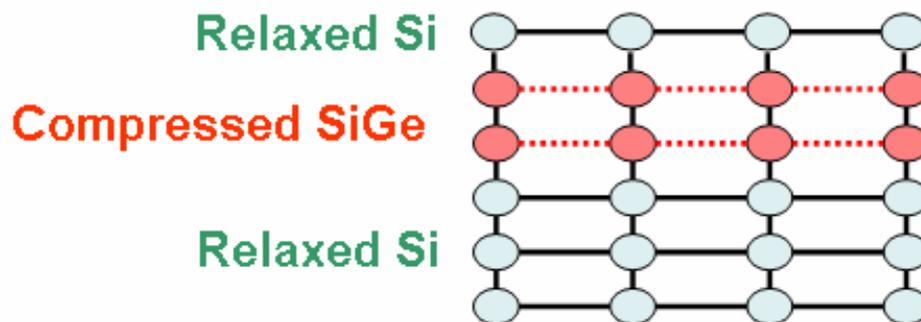
Zhang, et al, VLSI 2005



SSOI+SUR

Thean, et al, IEDM 200

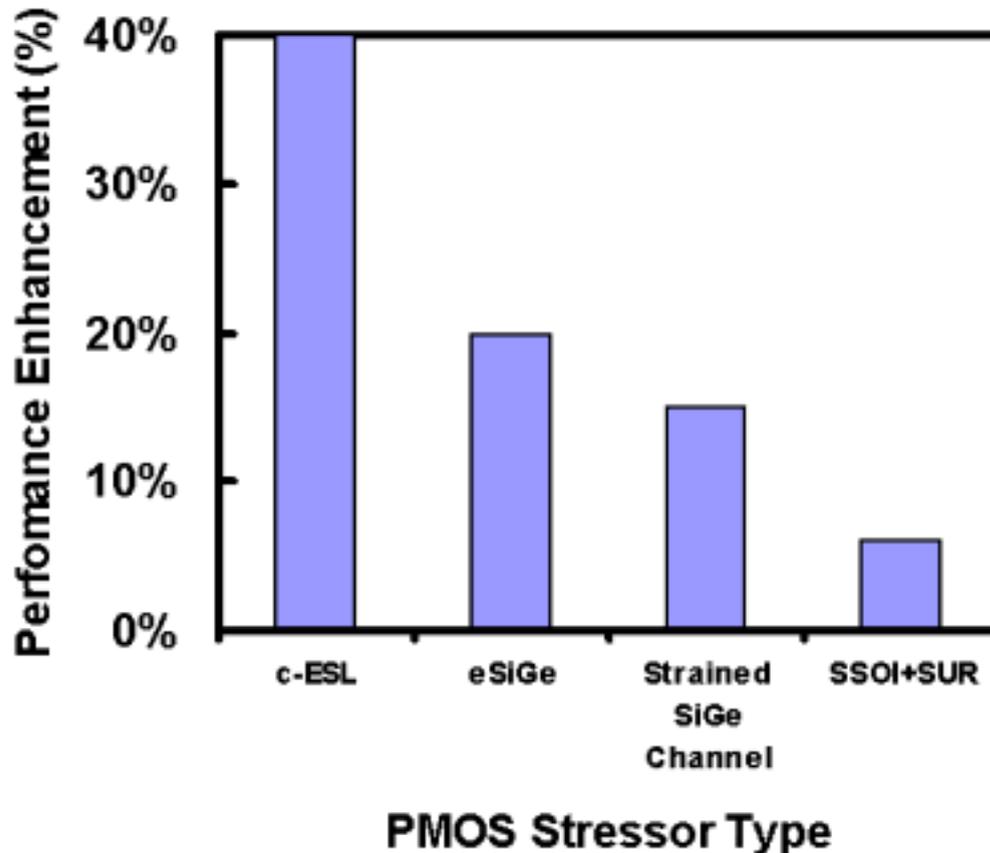
Biaxial



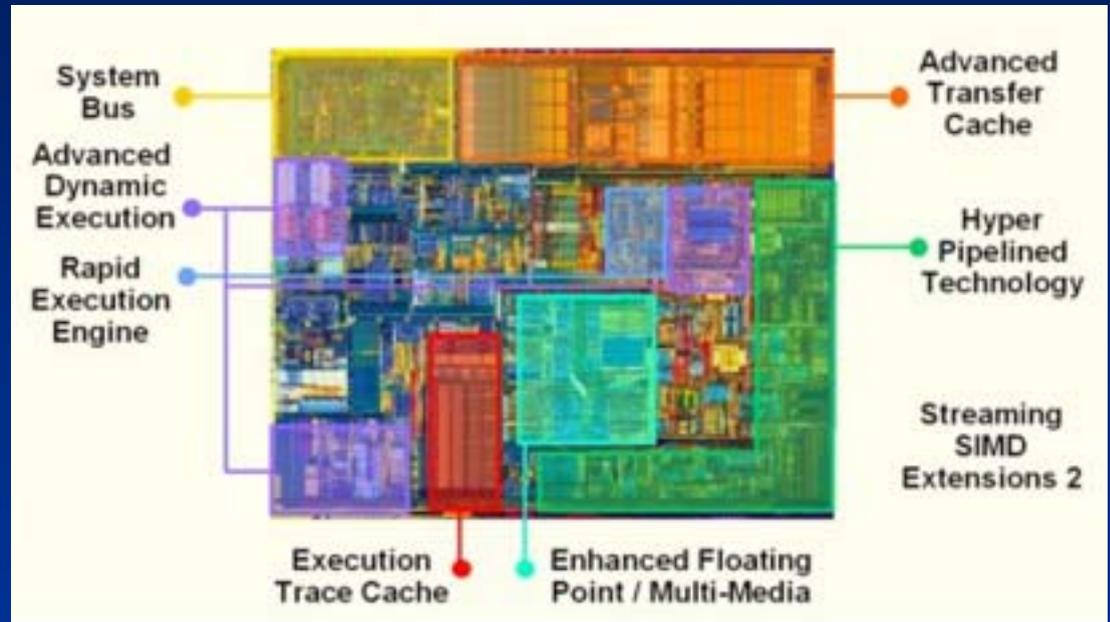
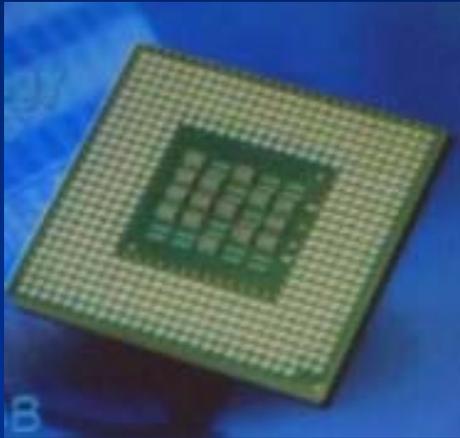
Colleart, et al, ESSDERC 2002

Strain Engineering

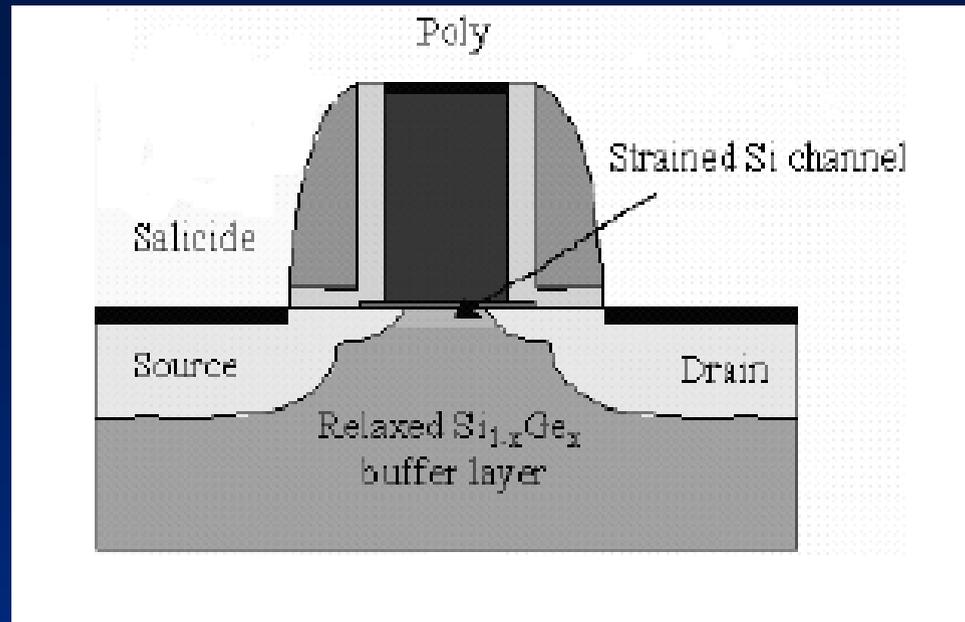
PMOS stressors



Intel于2002年8月发布了将应变Si技术应用在90nm CMOS技术上，正式宣告应变Si技术将进入量产，引起了IC业界极大关注。2005年完成90nm的Prescott Pentium 4 处理器,主频3.4GHz



Intel的Prescott Pentium 4 处理器

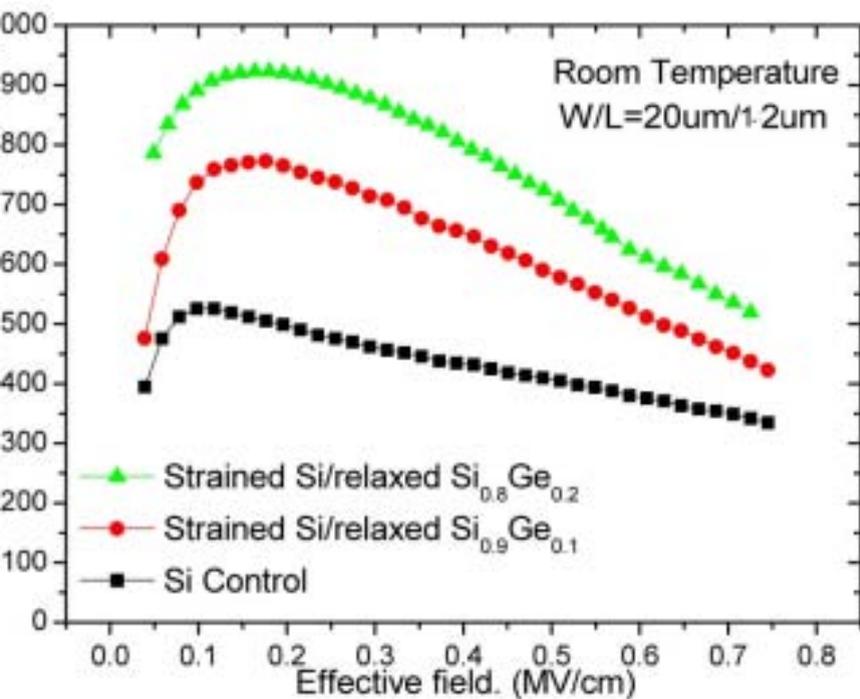


全局应变结构

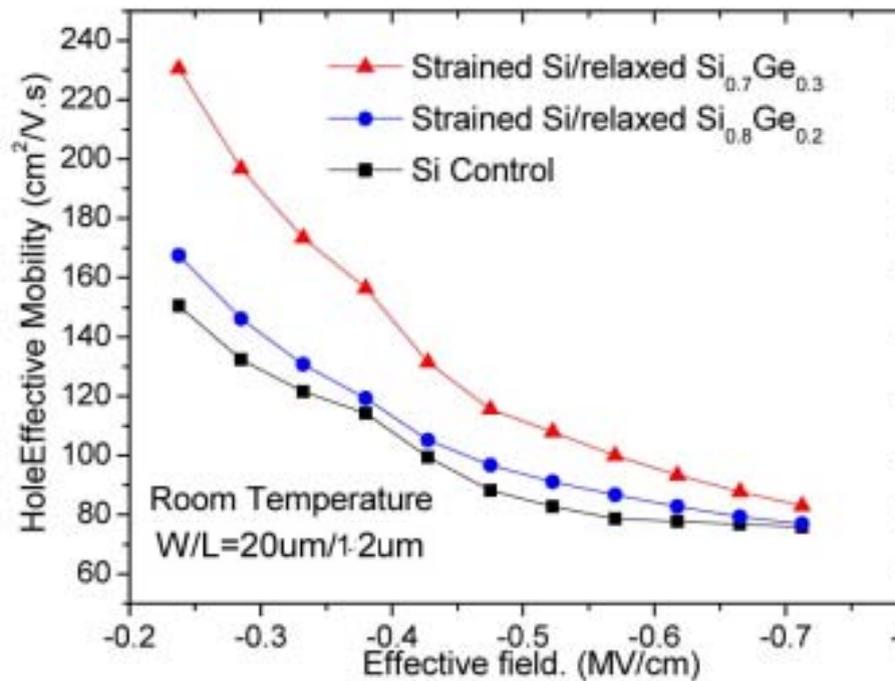
在SiGe上生长的Si层就会受到一个双轴张应力的作用，生长的SiGe高Ge组分层就会受到一个双轴压应力的作用。前者制造NMOS，后者制造PMOS。产生的应变改变了Si的能带结构，进而提高了载流子迁移率。

图示是一个在 $\text{Si}_{1-x}\text{Ge}_x$ 缓冲层上生长Si导电沟道的NMOS器件示意图。

国内最新研究进展

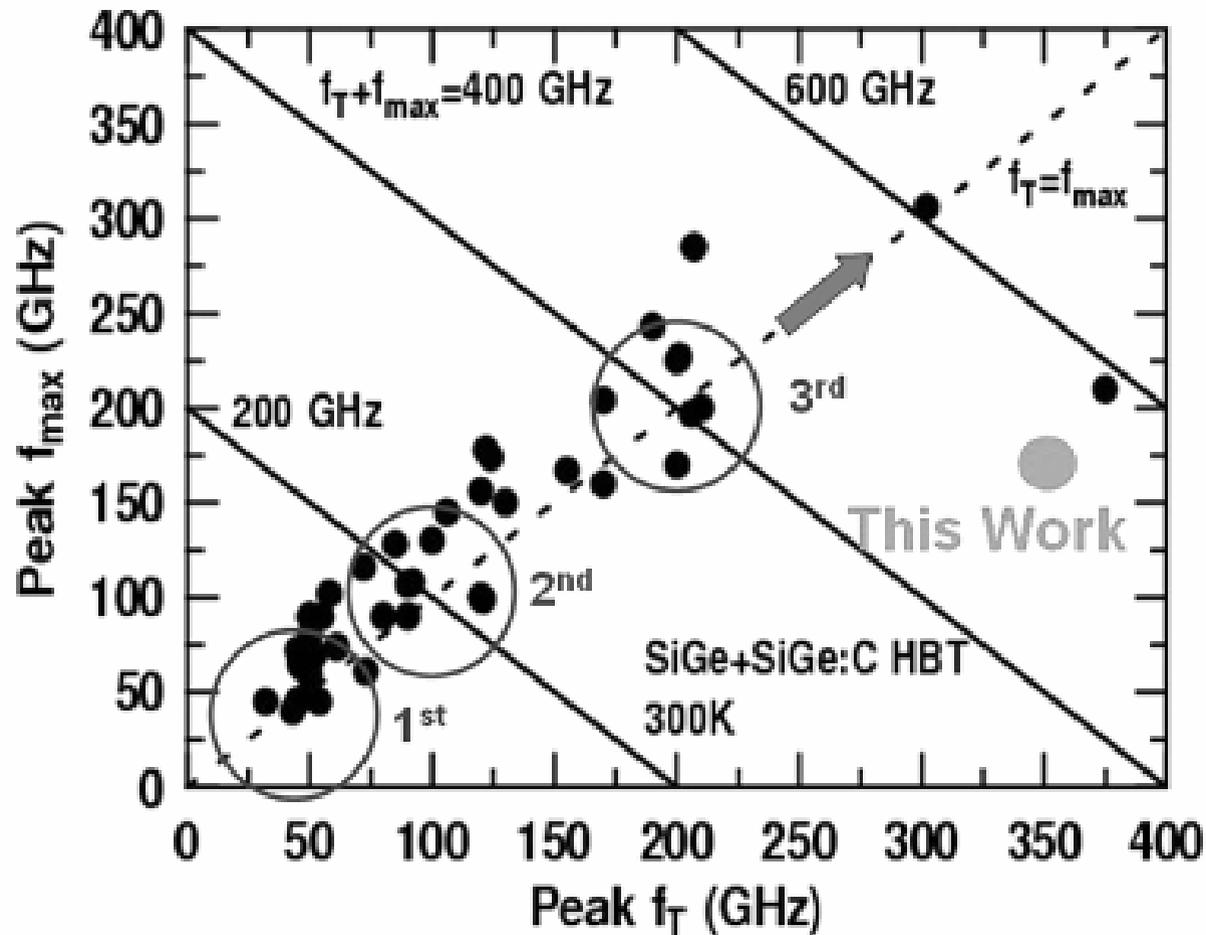


(a) NMOSFET



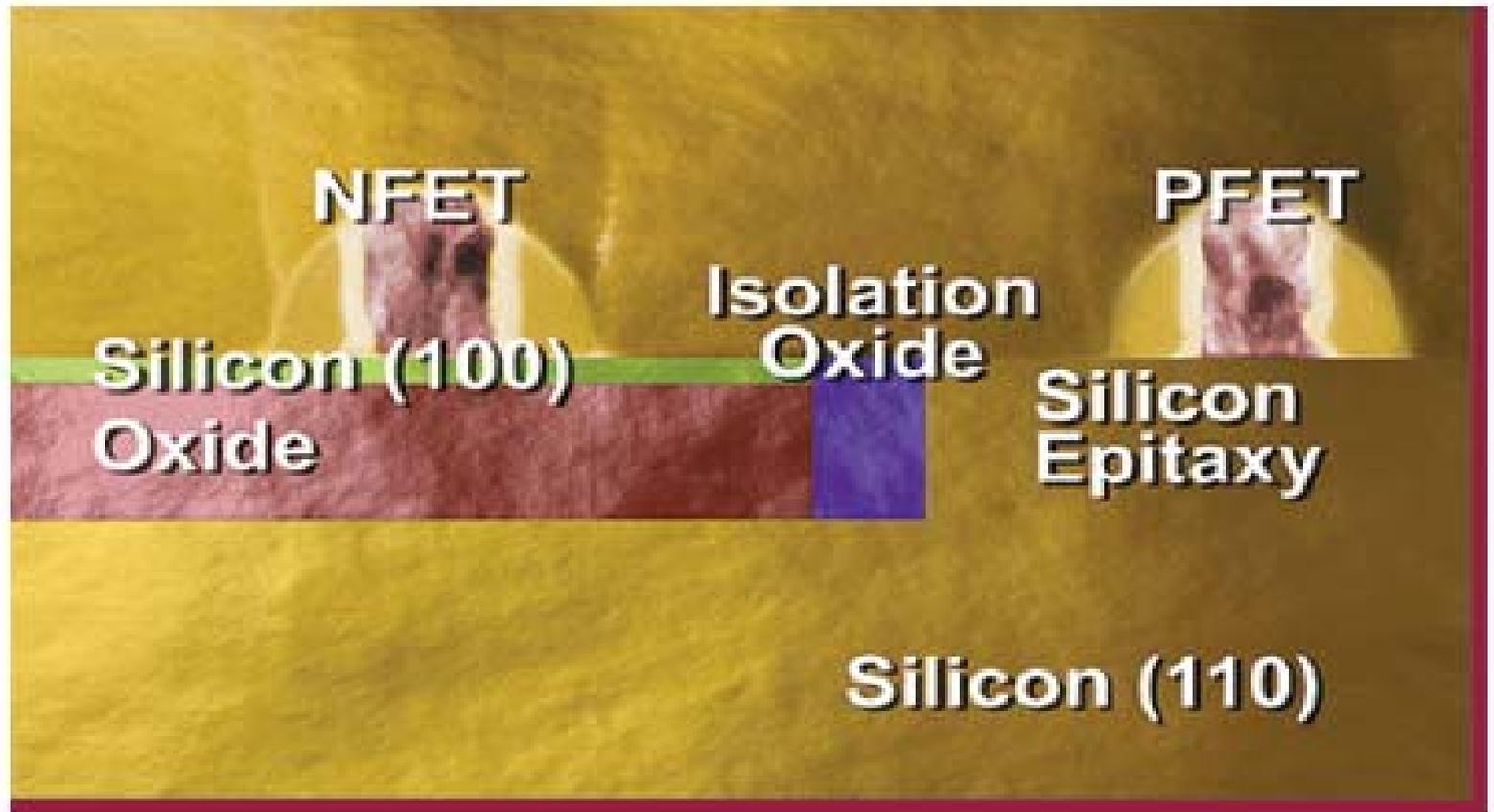
(b) PMOSFET

Strain Si + SiGe HBT BiCMOS



Comparison of SiGe HBT technology nodes in the f_T - f_{max} space.

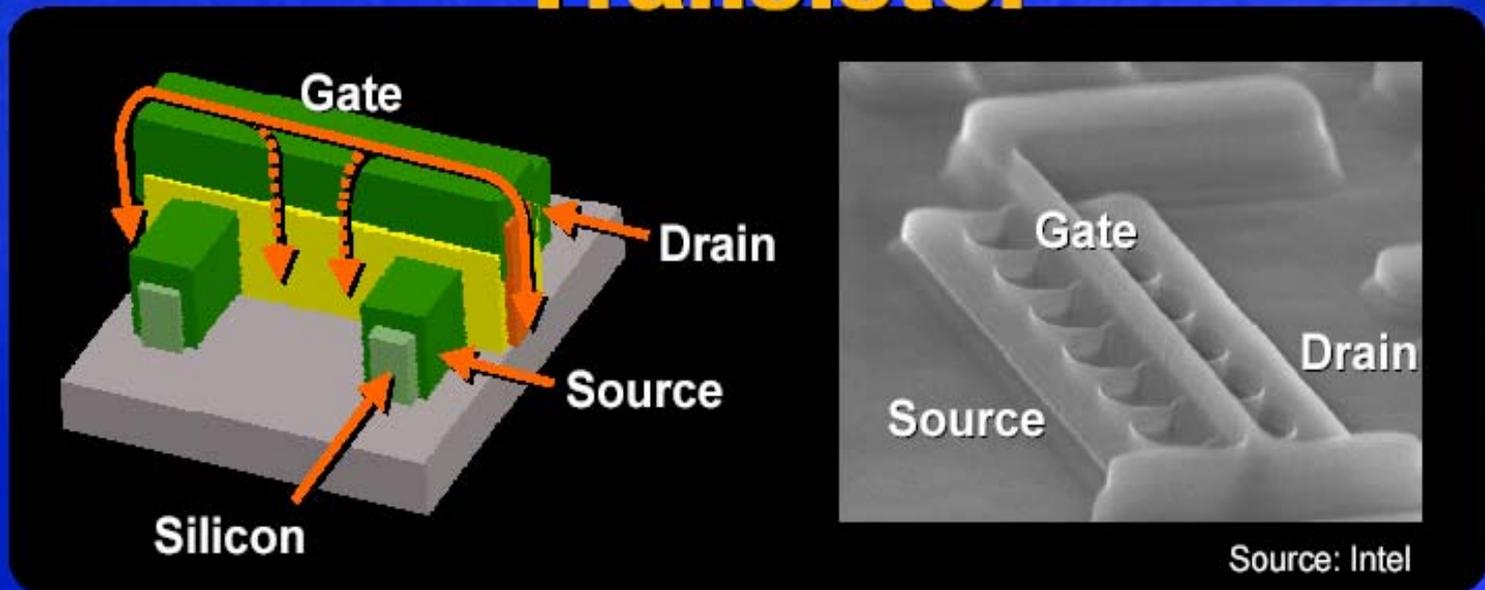
(二) 杂合晶向技术



杂合晶向技术能够在 (110) 晶向晶圆上制造出pFETs, 使得其运行速度提高了一倍。(来源: IBM)

Terahertz Electronics

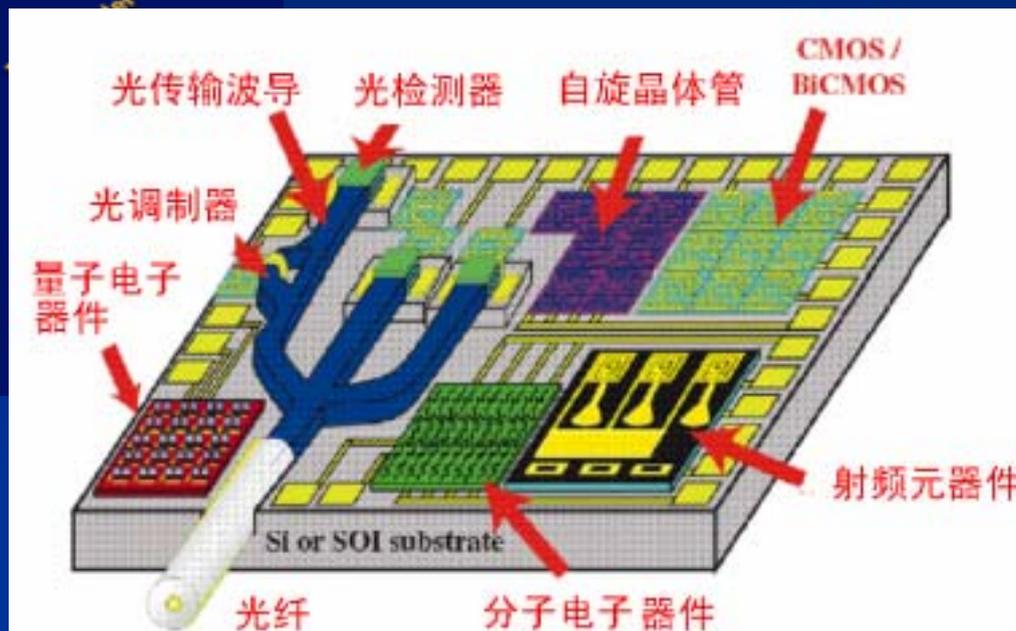
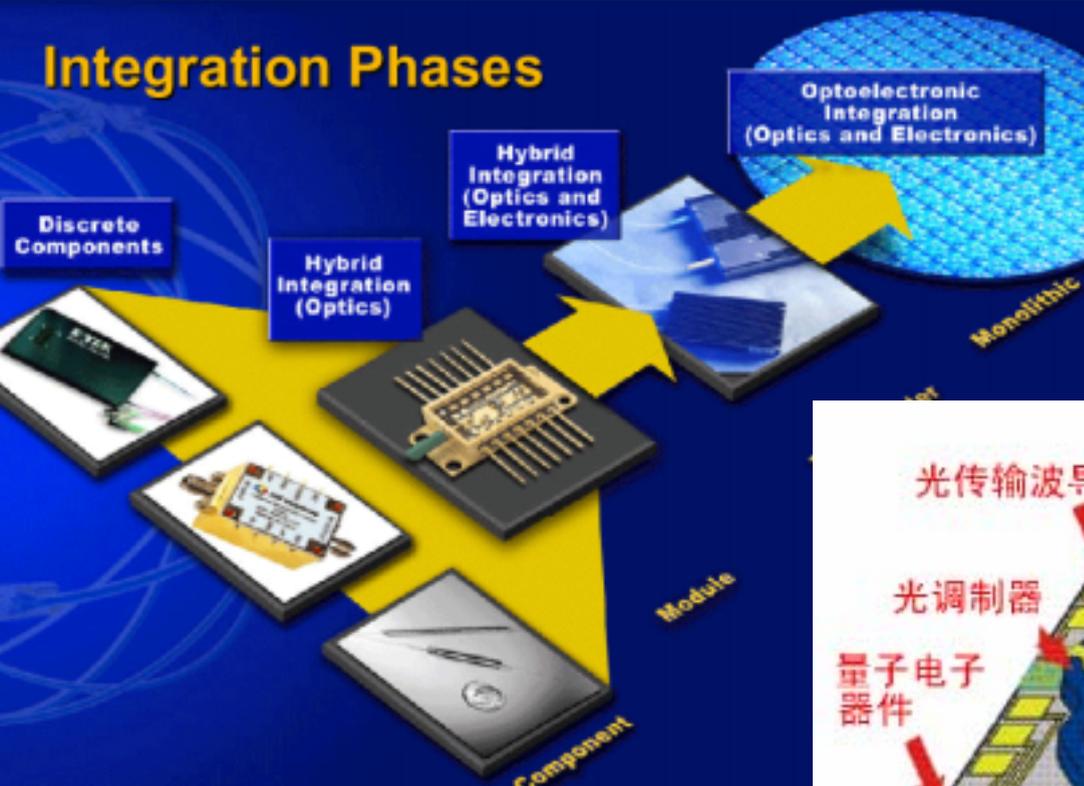
Experimental Tri-Gate Transistor



- Improved version of TeraHertz transistor
 - Better performance
 - Scalable to smaller sizes (low leakage)
 - Possible intercept towards end of decade?

光电集成技术

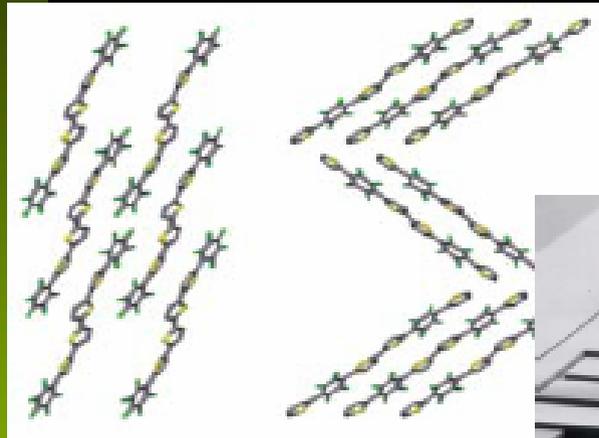
Integration Phases



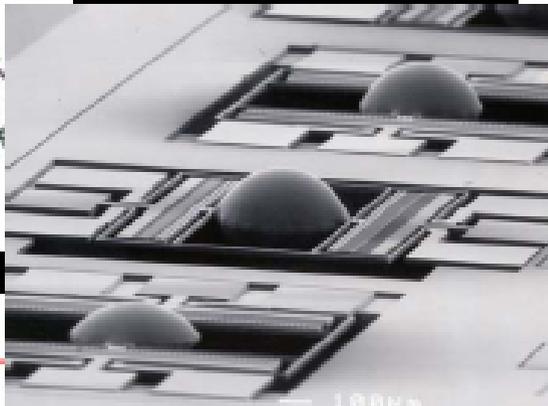
**(四) 依靠新型材料的进步
提高器件和电路的速度**

Transitioning to the Post-Silicon Age

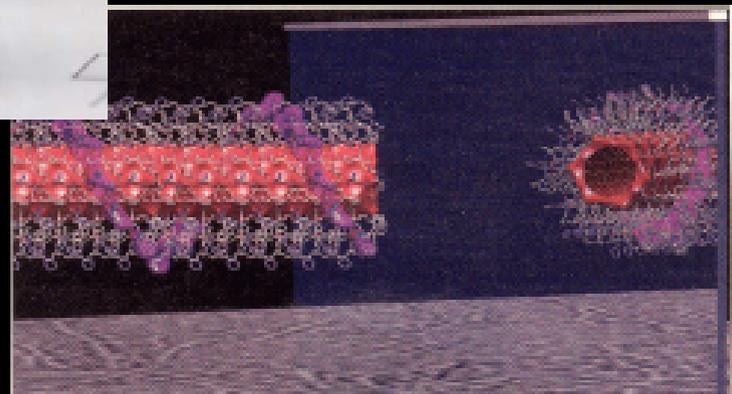
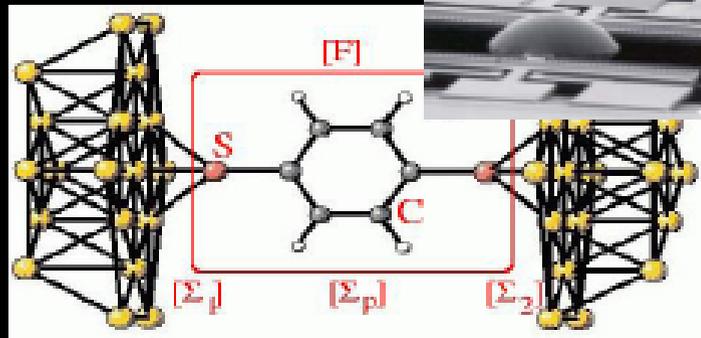
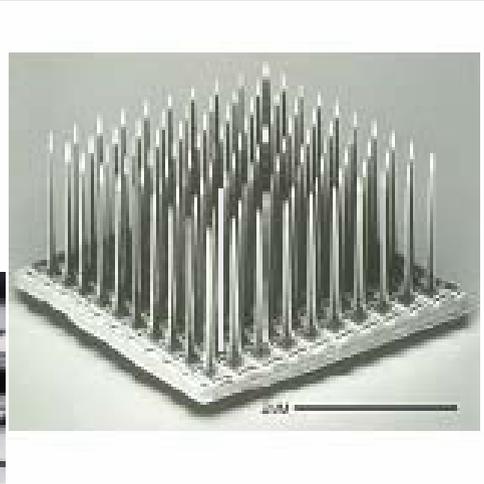
Organic



NanoOptics



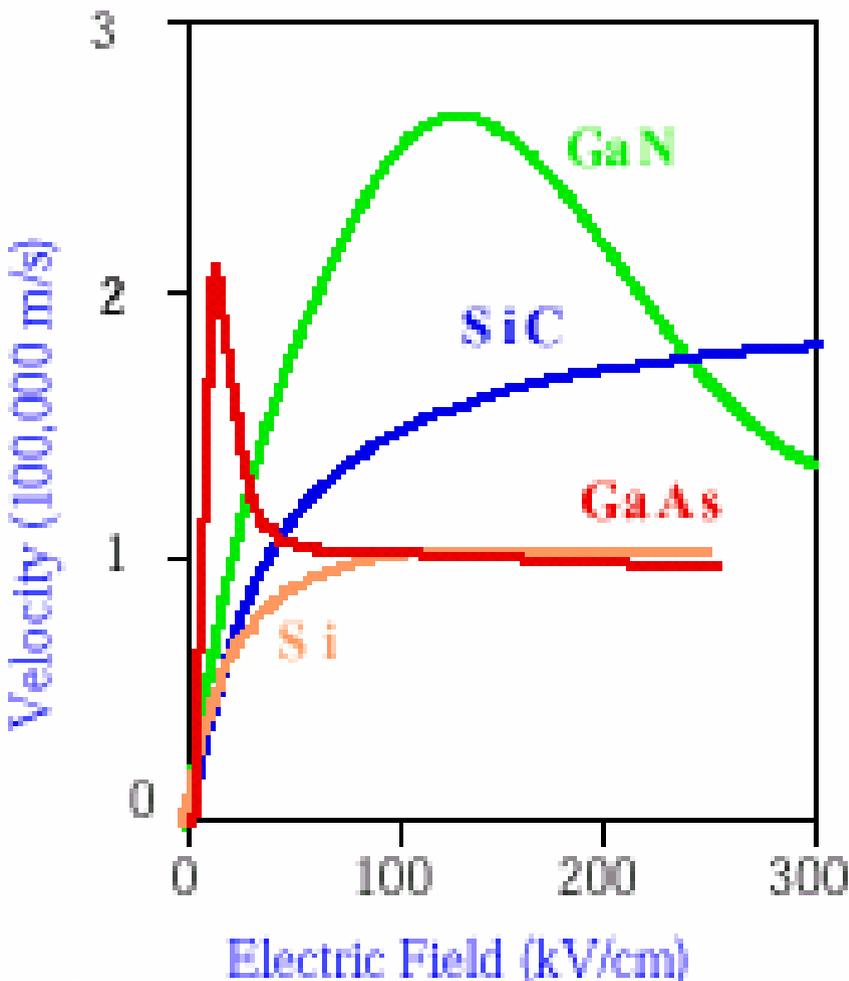
Nanotube



Molecular

Implementation platforms that work under very low SNR, are non-deterministic, unpredictable and unreliable...

High Drift Velocity and high mobility



$> 2,000 \text{ cm}^2/\text{V}\cdot\text{s}$ (300 K)

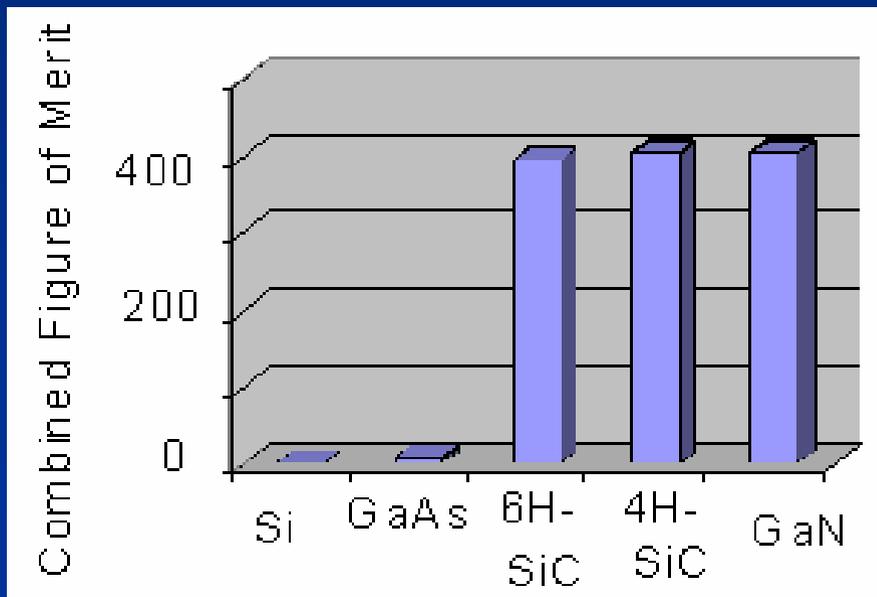
$> 10,000 \text{ cm}^2/\text{V}\cdot\text{s}$ (10 K)

R. Gaska, J. W. Yang,
A. Osinsky, Q. Chen, M. Asif Khan,
A. O. Orlov, G. L. Snider,
M. S. Shur, Appl. Phys. Lett.,
72, No. 6, pp. 707-709, Feb. 1998

超高速应用的综合品质因素

$$CFOM = \frac{\chi \epsilon_0 \mu v_s E_B^2}{\left(\chi \epsilon_0 \mu v_s E_B^2 \right)_{Si}}$$

其中， χ 为热导率， ϵ_0 为介电常数， μ 为迁移率， v_s 为电子饱和速度， E_B 为击穿电场强度。



不同材料特性比较

	Si	GaAs	SiC(4H)	GaN
禁带宽度(eV)	1.11	1.43	3.2	3.4
临界击穿电场 (MV/cm)	0.3	0.4	2	3.3
2DEG薄层电子 密度 (/ cm ²)	NA	4x10 ¹²	NA	20x10 ¹²
电子饱和速度 (cm/s)	1x10 ⁷	2x10 ⁷	2x10 ⁷	2.5x10 ⁷
电子迁移率 (cm ² /Vs)	1500	6000	800	1600

WBG Compound Semiconductors

Focus Areas

❖ **Material Technology**

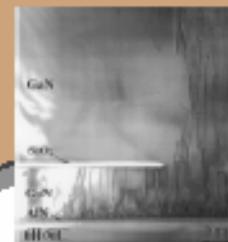
- **Bulk Crystal**
- **Epitaxial Materials**

❖ **Device Technology**

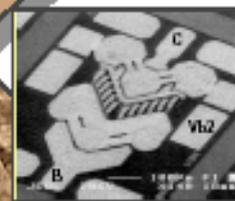
❖ **Thermal Control & Packages**



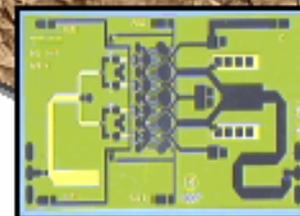
Advanced
Substrates
& Wafers



Epitaxial Materials



Electron Devices



Integrated Circuits



GaN在超高速器件方面的发展

- UCSB (USA)

$f_T=153\text{GHz}$, $f_{\text{max}}=230\text{GHz}$ ($L_G=0.10\mu\text{m}$)

- Rockwell (USA)

$f_T=123\text{GHz}$, $f_{\text{max}}=174\text{GHz}$ ($L_G=0.10\mu\text{m}$)

- Fraunhofer Institute (Germany)

$f_T=65\text{GHz}$, $f_{\text{max}}=140\text{GHz}$ ($L_G=0.18\mu\text{m}$)

- National Institute of Information and Communication Technology (Japan)

$f_T=163\text{GHz}$, $f_{\text{max}}=192\text{GHz}$ ($L_G=0.18\mu\text{m}$)

GaN/SiC材料生长设备

GaN材料外延设备：自主知识产权、运行良好的GaN材料生长用MOCVD-120和MOCVD-320系统；

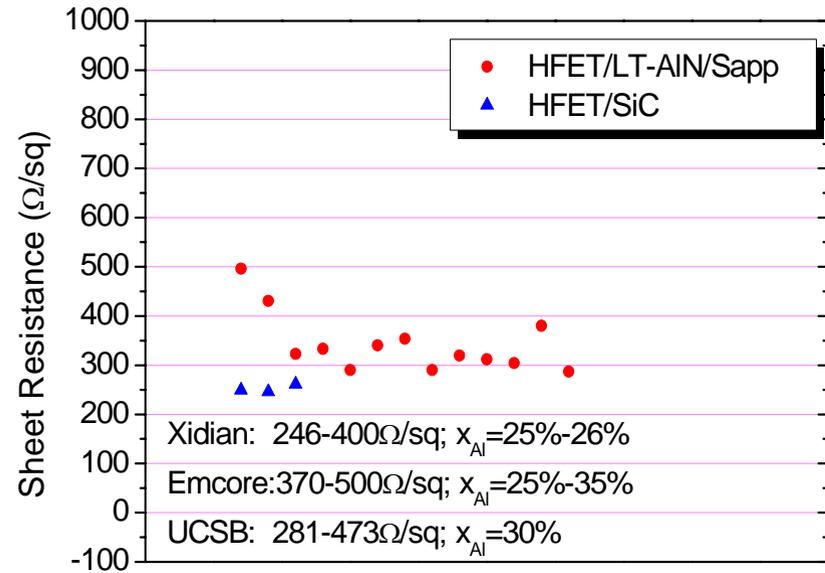
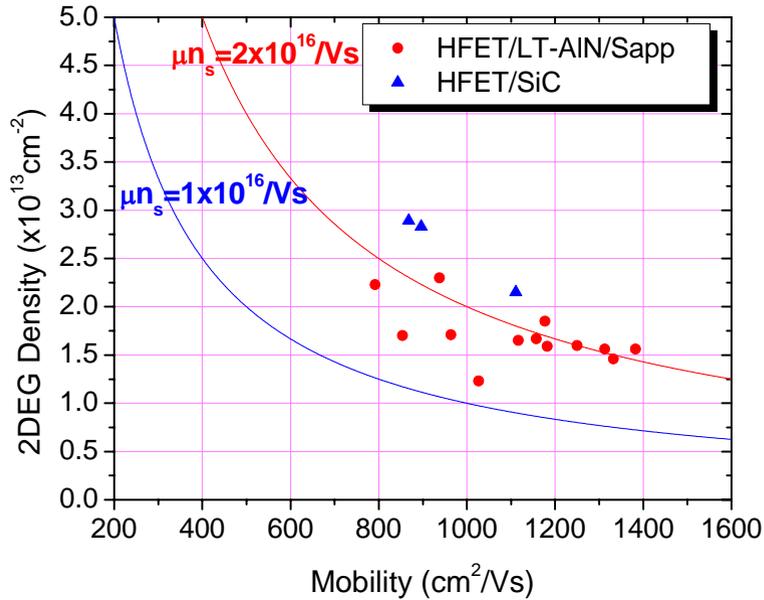
衬底制备：SiC CVD设备（瑞典Epigress VP508GFR），可同时生长六片2英寸SiC；



Layer structures of AlGaN/GaN Heterostructure



GaN异质结材料电特性（用于微波器件）



GaN异质结材料生长部分结果(2005-2006年)

- GaN异质结材料2DEG迁移率和面密度乘积高于 $2 \times 10^{16} / \text{Vs}$;
- 方块电阻均在246~400 Ω/sq 之间。

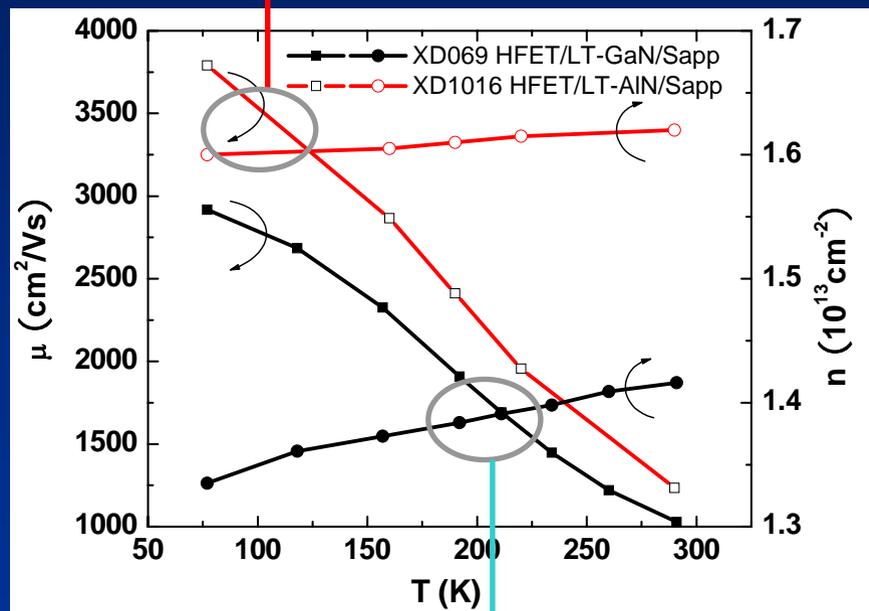
高性能AlGaN/GaN异质结材料

$$\mu_{300K}=1234\text{cm}^2/\text{Vs} ; \mu_{77K}= 3791\text{cm}^2/\text{Vs}$$

$$n_{300K}=1.62\text{E}13\text{cm}^{-2} ; n_{77K}= 1.6\text{E}13\text{cm}^{-2}$$

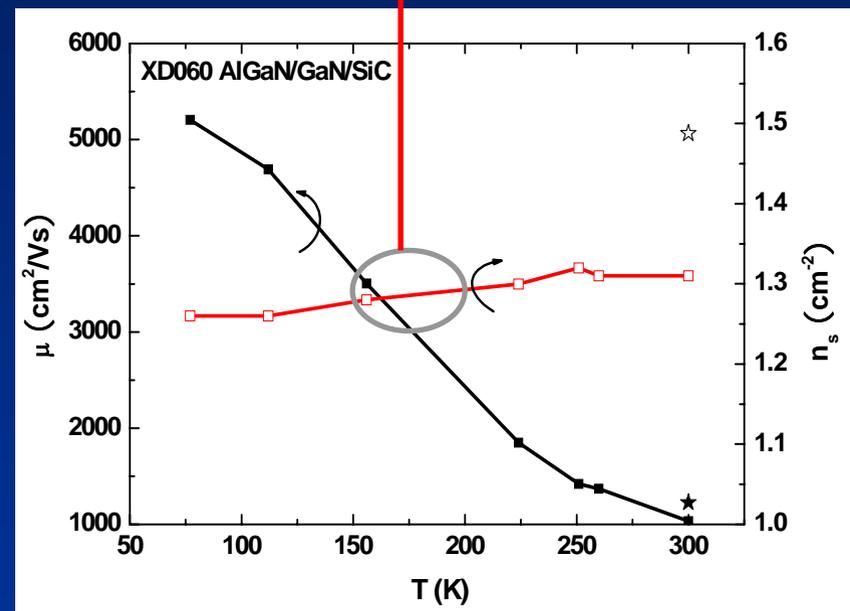
$$\mu_{300K}=1031\text{cm}^2/\text{Vs} ; \mu_{77K}= 5207\text{cm}^2/\text{Vs}$$

$$n_{300K}=1.31\text{E}13\text{cm}^{-2} ; n_{77K}= 1.26\text{E}13\text{cm}^{-2}$$

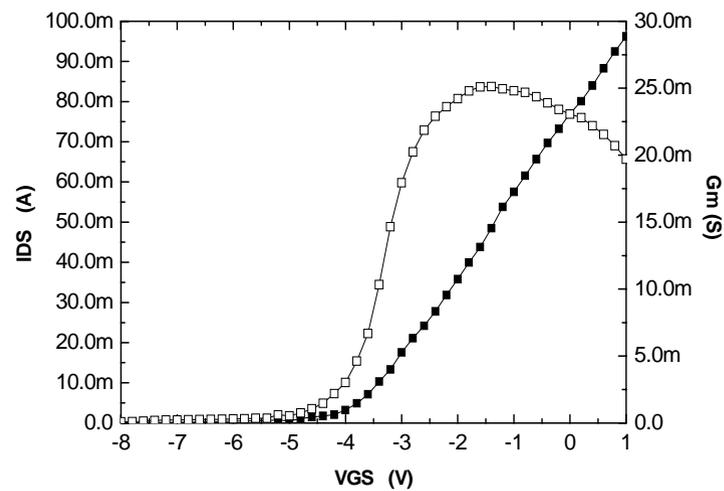
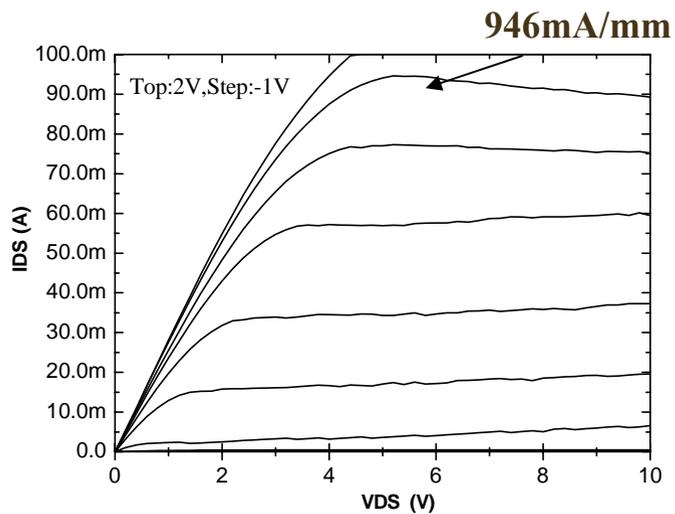
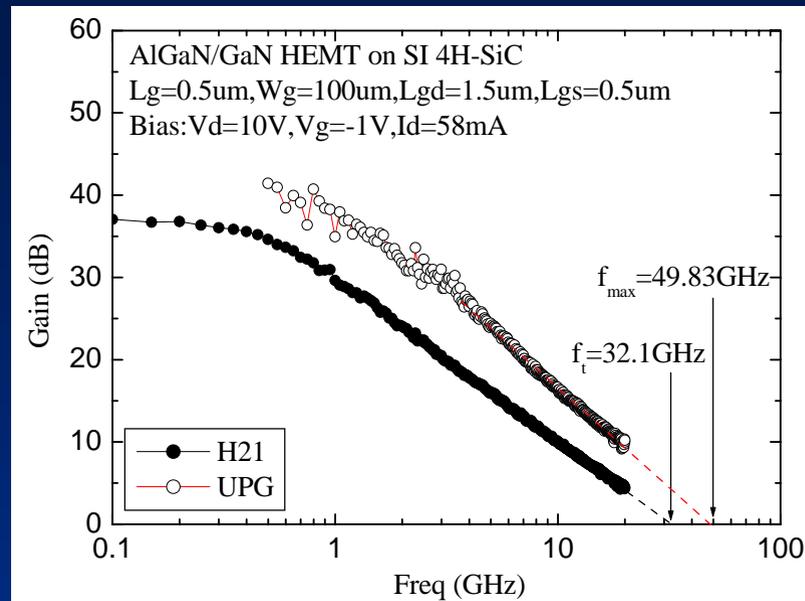
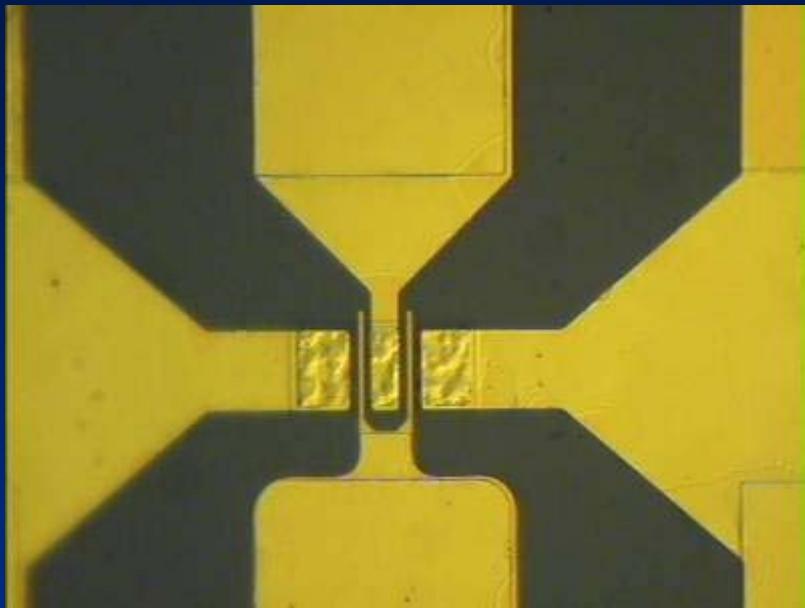


$$\mu_{300K}=1029\text{cm}^2/\text{Vs} ; \mu_{77K}= 2918\text{cm}^2/\text{Vs}$$

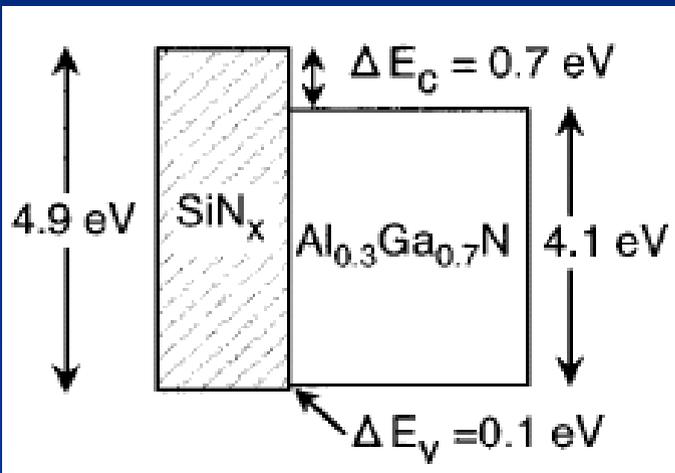
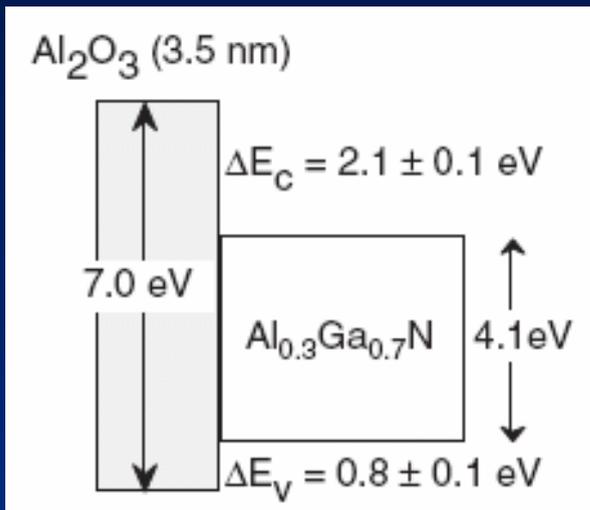
$$n_{300K}=1.42\text{E}13\text{cm}^{-2} ; n_{77K}= 1.34\text{E}13\text{cm}^{-2}$$



AlGaN/GaN HEMTs



原子层淀积Al₂O₃ / AlGa_{0.7}N高质量界面



	禁带宽度 (eV)	介电常数	击穿电压 (MV/cm)
Al _{0.3} Ga _{0.7} N	4.1	9-9.5	>5
PECVD SiO ₂	9	3.9	10
PECVD SiN	5	7	10
ALD Al ₂ O ₃	7-9	9-10	>10

原子层淀积 Al_2O_3 SEM, AFM分析



Fig.1. SEM观测到的 Al_2O_3 (3.5 nm) / AlGaIn表面，白色亮点为AlGaIn中缺陷



Fig.2. SEM观测到的 Al_2O_3 /Si表面，几乎没有缺陷

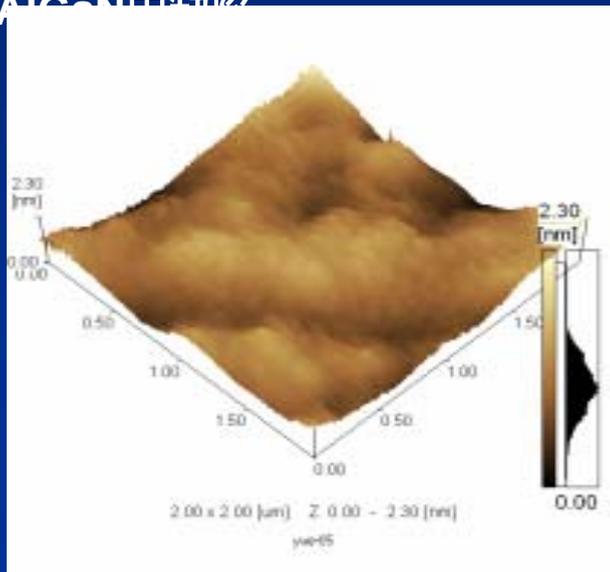


Fig.3. AFM观察到的AlGaIn/GaN表面三维图形(Rms=0.278nm)

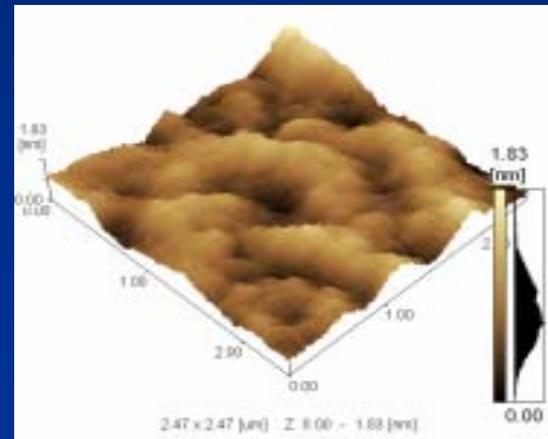
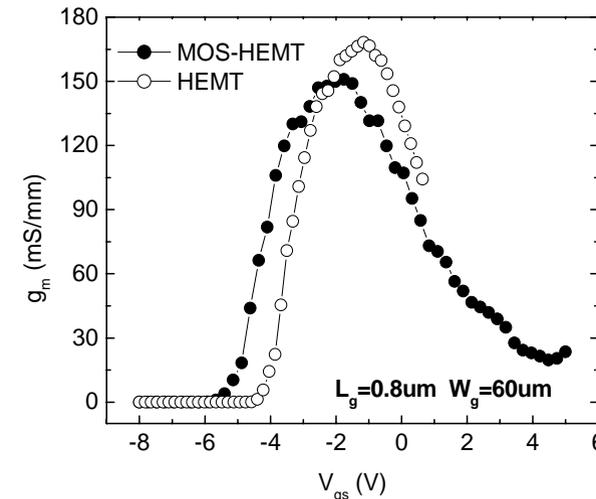
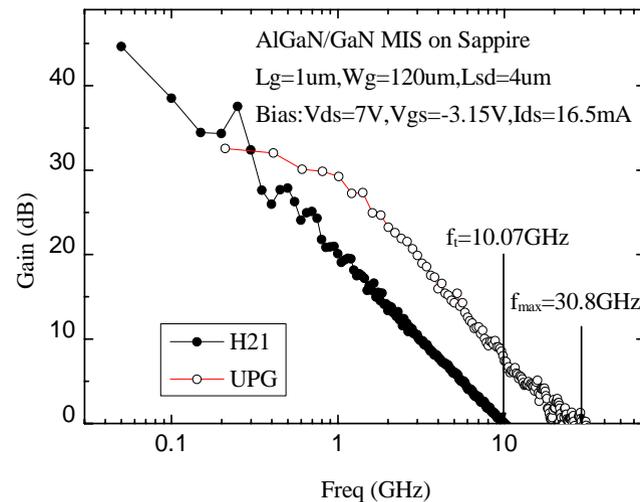
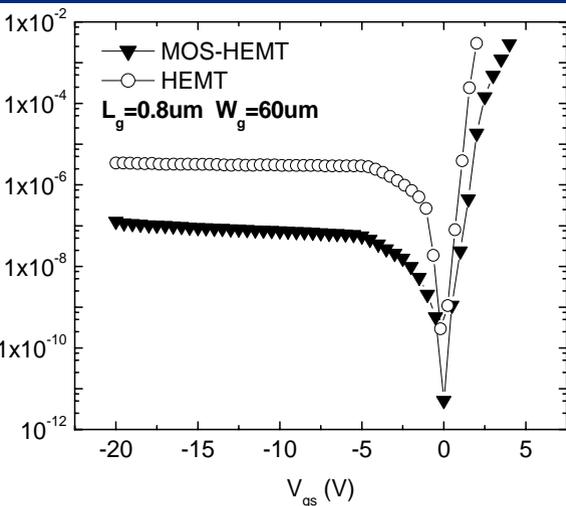
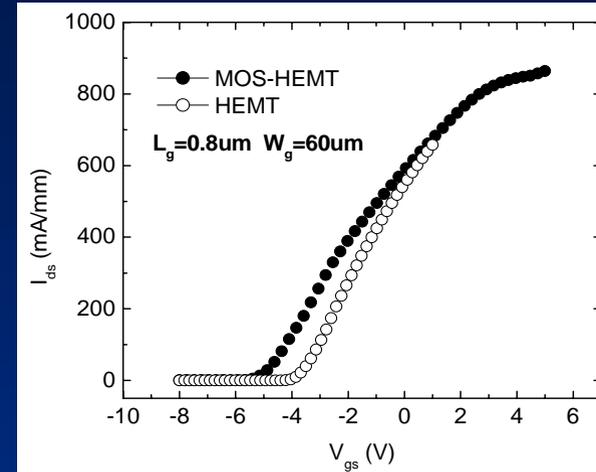
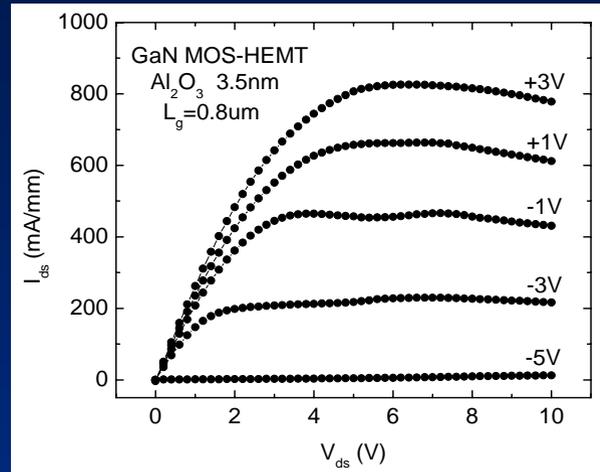
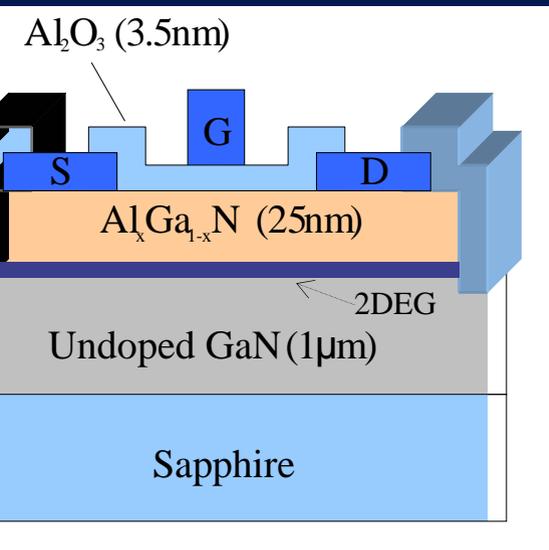
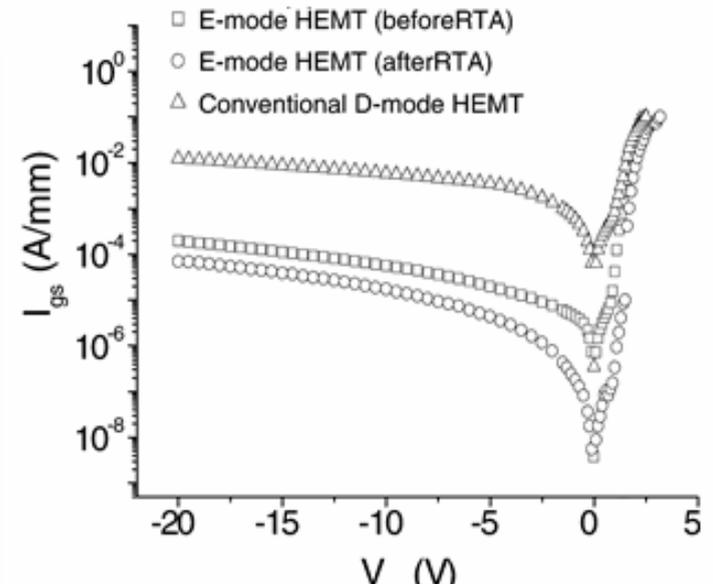
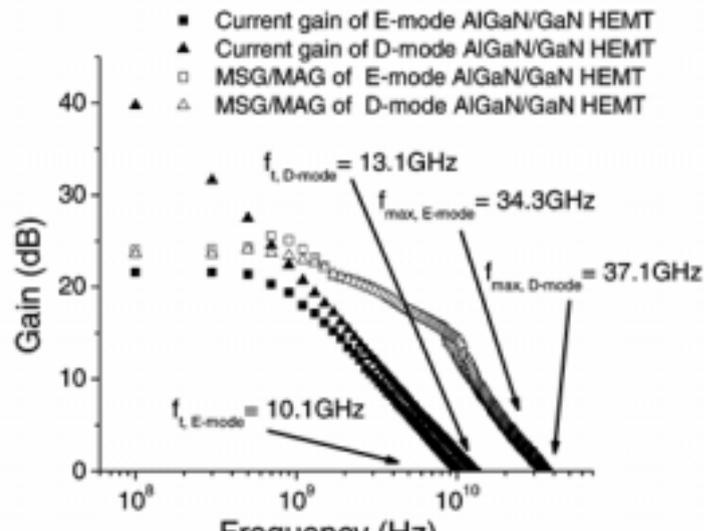
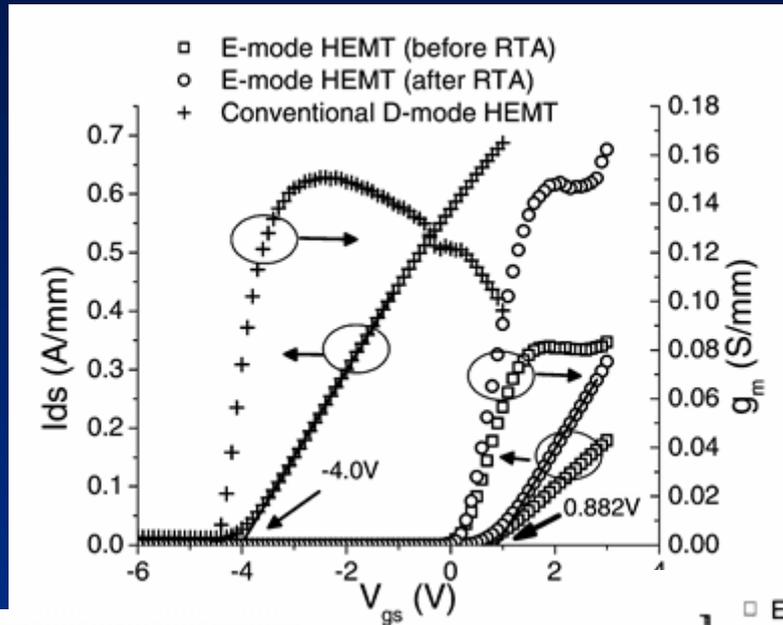


Fig.4. AFM观察到的 Al_2O_3 (3.5nm) / AlGaIn 表面三维图形(Rms=0.268nm)

GaN HEMT新结构 MOS-HEMT



增强型 (Enhancement Mode) HEMT



结 论

超高速是集成电路追究的主要目标，高速宽带的信息处理是主要的应用驱动。

- 依靠缩小线宽提高速度越来越困难，还在不断发展
- 设计技术是提高速度的有效方法，空间还很大
- 新型材料是增强速度的有效手段，潜力无限

实现基于材料和器件的设计技术

基于设计的器件和材料技术

技术和学科高度融合和互动

谢谢！